

The AR250

A New Architecture for Ray Traced Rendering



SIGGRAPH '99 – Slides

Architecture overview

- AR250 Rendering Processor
- RenderDrive Network Appliance
- How and why it works
 - Problems with Parallelism
 - The ART Model
 - Main AR250 Data Flows
 - AR250 Statistics
 - Analysis

Performance

- Functionality
- Rendering Speed



AR250 Rendering Processor



RenderDrive Network Appliance





Problems with Parallelism

- Data distribution
- Load balancing
- Scalability of calculation
- Complexity



The ART Model

- Hardware intersection pipeline
- Ray-parallel data distribution
- Broadcast parallelism of geometry
- Hierarchical geometry
- Distributed concurrent shading
- Vector parallel programmable shading acceleration



Main AR250 Data Flows





AR250 Statistics

- 0.35um drawn, LSI Logic G10 silicon process
- 650K gates, 106mm² die
- Custom RISC processor core
- 32, single-stage, 32 bit IEEE compatible floating-point units
- Multi-dimensional noise, square root and trig. functions
- 50 MHz operation



Analysis

- Load balancing through fine-grain parallelism
- Efficient data distribution by caching rays locally and broadcasting geometry
- Scalability by performing whole rendering calculation, including shading.
- Low complexity programming model by support for programmable shading in silicon



Functionality

Current

- Full shading model
- Full ray-traced:
 Camera motion blur
 Depth of field
 Area lights
 Volumes

Planned

- Global illumination
- Completion of RenderMan support



Rendering Speed

Scalability



Hebe mirror (1322 x 2000) RenderDrive (16 x AR250) BMRT (PII - 333)

0 hrs 13 min 2 sec 22 hrs 8 min