Falanx Microsystems

Company Overview

- Design and license silicon graphics IP cores targeted at mobile phones and system-on-chip
- Core Competencies
  - Computer Graphics Architectures and Algorithms
  - Hardware Description Languages and Tools
  - Software Design and Development
- Norway / US
  - Trondheim – the technology capitol of Norway
  - Falanx Inc.
- Zoran first licensee

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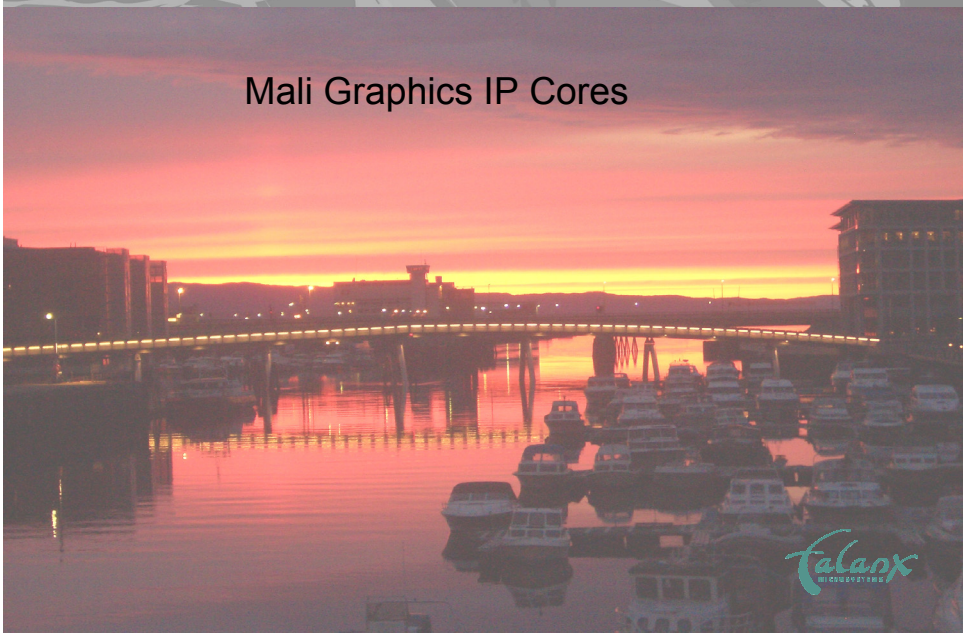
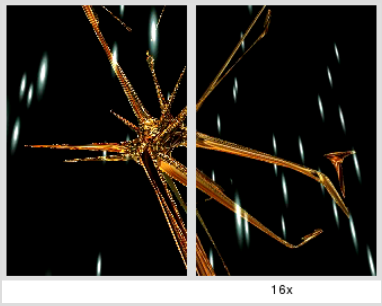


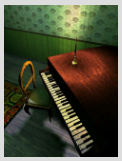
Overview

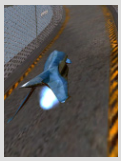
- Mali Graphics IP Cores
  - First implementation of Falanx' architecture
  - Scales with the OpenGL®ES road-map
  - 4X Full Scene Anti-Aliasing Standard
    - Up to 100-200MPix / s dependent on texturing, etc.
    - No measurable decrease in performance or increase in bandwidth usage.
  - 16X Full Scene Anti-Aliasing Option

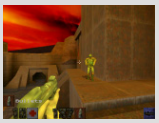
Image Quality

- Anti-Aliasing Important For IQ
  - Small displays *can* look brilliant
- Several algorithms, but
  - Unacceptable increase in memory BW / power
  - Unacceptable performance hits
- No compromise

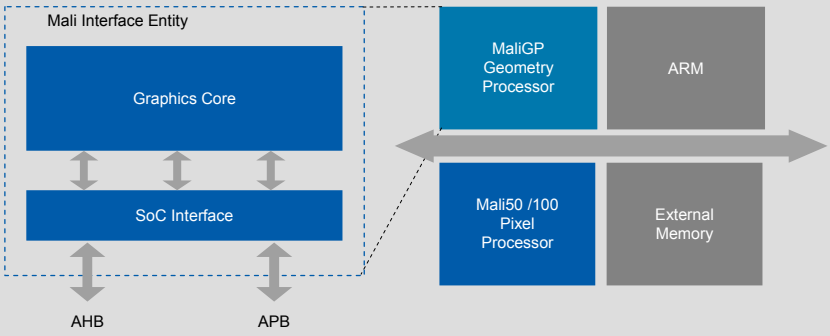








Block Diagram



Current Products

	Mali100+G	Mali50+G	Mali100	Mali50
Max Clock	180MHz	180MHz	180MHz	180MHz
M Pix / s	180	90	180	90
M Tri / s	5	2.5	*CPU*	*CPU*
Total Area	5 mm^2	4 mm^2	3,5 mm^2	2 mm^2

- Performance given with 4X FSAA Mode
  - Bilinear single texture
- Area given with Free Artisan TSMC 130nm library
  - Includes scan, clock gating and SRAMs

Rich Feature Set

Key Features
- 4X FSAA Standard Operation
- 16X FSAA at your request
- Video Primitives Acceleration
- Texture Compression (FLXTC)
- OpenGL ES Feature Set and more

System features
- 16 / 32 bit frame buffer
- Max. Resolution 2048x2048
- Autonomous Frame Rendering
- Memory Management Unit

Other Hardware Accelerated Features - High lights
- Points / Lines / Triangles / *Quads*
- Flat / Gouraud Shading
- Point / Bi-linear / Tri-linear Texturing
- Multi texturing
- Auto Mip Map Generation
- Dot3 Bump Mapping
- Flexible Texture Input formats
- Aggressive Z Tests
- Triangle Setup
- 2D / Point / JSR184 Sprites
- Anti-aliased font rendering
- Bitblt / ROP3/4
- *Vertex Shader 2.0*
- *4-bit Stencil Buffers*
- *Specular Color / Color Sum*
- *Render To Texture w/ AA*
- *Matrix Palette Skinning*
- *DCT / iDCT*

Silicon IP Cores

- Soft Cores are Challenging because of
  - Tool Chains, Coding and design styles
    - Requires extensive chip design and HDL knowledge
  - Different System-on-Chip Architectures and OSs needs special attention
    - For maximum performance software and hardware must be designed together
    - Different memory controllers, bus latencies and bus arbiter implementations affects the graphics system

Silicon IP Cores

- FHDL – Falanx HDL
  - Compiles to different targets (Verilog, VHDL, ++)
  - Verified and proven through several different HDL simulators, synthesis tools, back-end flow
  - Enables quick and painless transition to new tools, embedding of “special requests” and coding styles
- Software Development
  - ANSI C or die
  - ARM and OS optimizations give an edge
- Falanx IP cores:
  - Affects the SoC design as little as possible
  - Are as pluggable, re-usable and scalable as possible

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