3D Graphics LSI Core for Mobile Phone “Z3D”

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Abstract

• Architecture of 3D graphics accelerator on mobile phone

D504i Mobile Phone Mounting Z3D
Outline

• Background
• Development Concept
• System Architecture
• Performance
• Power Consumption
• Conclusions
• Demos
Graphics System Trend

• Dedicated Machine
  – Flight Simulator/CAD system using general purpose computer systems
  – Huge system

• UNIX workstation
  – Several boards

• PC
  – PCI/AGP board/LSI Chip

• Mobile Phone/Terminal
  – Small LSI Core/Low Power Consumption
Mobile Phone’s Display Trend

• High Quality LCD
  – Full Color
    • 260K colors, (R,G,B)=(6,6,6) bits
  – Large size
    • 2.1 inches ➔ 2.2 inches
  – High Resolution
    • 132x176 ➔ QVGA(240 x 320)

• From Wireless Phone to Multi-Media Terminal
  – Same way PC traced
Contributions

- First attempt to have implemented a graphics accelerator on mobile phone
- Geometry engine architecture
  - At low clock frequency
  - Animation functions except for low level geometry processing
- Rendering pipeline architecture running with low power consumption
- Total system architecture including JAVA-API and content manufacturing
Development Concept

• More than 7fps animation
• Low power consumption
• Low clock frequency
• Small LSI core
• CPU power free
• Open API architecture
  – Easy content development
  – To use commercial modeler
3D Graphics Applications

- Character animation
- Game
- Walk through
- 3D icons
Functions

- **3D graphics**
  - Smooth shading
    - Multi-lights (up to 8 lights)
    - Parallel/point/corn lights
    - Specular high light
  - Texture mapping
    - Perspective error correction
    - Bilinear interpolation
  - Pixel processing
    - Fog
    - Alpha blending
    - Anti-alias line

- **2D acceleration**
System Architecture

- Traditional rendering pipeline
  - Geometry engine/Rendering engine/Pixel engine

- Geometry engine
  - CPU power is low
    - CPU has no floating point processing unit and runs at low clock frequency

- All graphics memories are implemented
  - Display list buffer
  - Texture memory
  - Frame Buffer (Z buffer, Stencil buffer)

- Gated clock
Hardware Configuration
Memories

• Display list buffer
  – 24 bits x 40KW = 120 KB

• Texture memory
  – 13 bits x 256 x 128 = 53 KB

• Frame buffer
  – (R,G,B) = (6,6,6) bits, Z = 12 bits, Stencil bits = 2 bits
  – 32 bits x 132 x 176 = 93 KB
Geometry Engine Architecture

• Micro-code programmable processor like DSP
  – High performance arithmetic processor
  – Manage the data in the display list buffer

• Two parallel SIMD type floating point processor
  – Two 24-bit floating point processing units
    • Because of a small screen
    • 1-bit sign, 7-bit exponent, 16-bit mantissa
  – A 24-bit integer processing unit

• Special floating point processing units
  – Normalization unit \((1/(\text{square root}(x)))\)
  – Power unit \((x^y)\)
  – Clip tester
GE Configuration

Host Bus

Host Bus-IF

Address Generator

Sequencer

Instruction Memory

LMI

LMF1

LMF2

LUTF

IPU

Clip Tester

FPU1

FPU2

Normalization

Power

Rendering Engine-IF

To Rendering Engine

To Display List Buffer
Instruction Pipeline of GE

Instruction n
F  D  MR  E  WB

Instruction (n+1)
F  D  MR  E  WB

Instruction (n+2)
F  D  MR  E  WB

\[1\text{clk}\]

F : Fetch
D : Decode
MR : Memory Read
E : Execution
WB : Write Back
GE Micro-code

• Geometry processing
  – Subset of OpenGL
    • 53 functions (vs. 350 functions of OpenGL)

• Animation processing
  – Key frame animation
    • Color animation, Location animation, Scalar animation, Rotation animation
    • Described by VRML
    • Can reduce the data
  – Skinning
GE Features

- Compact configuration
  - 24-bit floating point processing
  - The space of instruction memory and display list buffer are limited
- Two parallel SIMD type floating point processing
  - 120Mflops at 30 MHz
- Special arithmetic processing unit
  - Normalization, power, clip test
- Micro-code control
  - Geometry processing
  - Key frame animation
  - skinning
Display Sample

- Shading
- Texture mapping
- Multi lights
- Alpha blending
Performance

• Geometry performance
  – Up to 185K vertex/sec
• Pixel performance
  – Up to 5M pixel/sec
• At 30MHz
Actual Performance

Performance curve at pipeline mode, four-vertex triangle strip mode
LSI Implementation

- 360K gates logic and 2.3Mbits SRAM
- 30 mm$^2$ using 0.18 um process
  - 11 mm$^2$ for logic
  - 19 mm$^2$ for SRAM
Gated Clock

• General way to reduce power consumption
• Two types
  – Functional block base
    • Clock supply is separated for 3D pipeline, 2D engine and LCD-controller
    • Only one clock is activated
      – When 3D pipeline is working, clocks are not supplied to 2D engine and LCD controller
  – 3D pipeline base (Step mode)
    • Divide 3D pipeline to three portions
      – Geometry engine/set up engine/others(Raster engine, Texture engine, Pixel engine)
      – Clocks are supplied and turned off sequentially and automatically
# Pipeline Mode vs. Step Mode

## Pipeline Mode

<table>
<thead>
<tr>
<th></th>
<th>Vn</th>
<th>Vn+1</th>
<th>Vn+2</th>
<th>Vn+3</th>
<th>Vn+4</th>
<th>Vn+5</th>
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</thead>
<tbody>
<tr>
<td>Geometry Engine</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Set Up Engine</td>
<td></td>
<td>Vn</td>
<td>Vn+1</td>
<td>Vn+2</td>
<td>Vn+3</td>
<td>Vn+4</td>
</tr>
<tr>
<td>Raster Engine</td>
<td></td>
<td></td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>Texture Engine</td>
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<td></td>
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<tr>
<td>Pixel Engine</td>
<td></td>
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</tr>
</tbody>
</table>

Clock is supplied

## Step Mode

<table>
<thead>
<tr>
<th></th>
<th>Vn</th>
<th>Vn+1</th>
<th>Vn+2</th>
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</thead>
<tbody>
<tr>
<td>Geometry Engine</td>
<td>Vn</td>
<td></td>
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</tr>
<tr>
<td>Set Up Engine</td>
<td></td>
<td>Vn</td>
<td>Vn+1</td>
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<tr>
<td>Raster Engine</td>
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<tr>
<td>Texture Engine</td>
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<tr>
<td>Pixel Engine</td>
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</table>

Clock is not supplied
Power Consumption

Sample Applications

<table>
<thead>
<tr>
<th>Application</th>
<th>(a)</th>
<th>(b)</th>
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<tbody>
<tr>
<td>Vertex count</td>
<td>4690</td>
<td>1717</td>
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<tr>
<td>Polygon count</td>
<td>2134</td>
<td>973</td>
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<tr>
<td>Average pixel count per polygon</td>
<td>6.3</td>
<td>49.8</td>
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</table>

<table>
<thead>
<tr>
<th></th>
<th>Power Consumption</th>
<th>Performance</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(a)</td>
<td>(b)</td>
</tr>
<tr>
<td>Pipeline mode</td>
<td>66 mW</td>
<td>66 mW</td>
</tr>
<tr>
<td></td>
<td>8.5 fps</td>
<td>19.1 fps</td>
</tr>
<tr>
<td>Step mode</td>
<td>38 mW</td>
<td>38 mW</td>
</tr>
<tr>
<td></td>
<td>8.0 fps</td>
<td>17.3 fps</td>
</tr>
</tbody>
</table>
Study of Power Consumption

• Content designers like “1 light with texture” mode
  – Geometry performance is bottleneck
    • 80 Kvertex/sec

- Geometry Engine
  \[ V_n \quad V_{n+1} \quad V_{n+2} \]
- Set Up Engine
  \[ V_n \quad V_{n+1} \]
- \{ Raster Engine, Texture Engine, Pixel Engine \}
  \[ V_n \quad V_{n+1} \]

• Power consumption was reduced 43%
• Performance reduction was 6% in application (a) and 10% in application (b)
Software Configuration

Network
- VRML2.0 File
- VRML Converter
- Dedicated Converter

SW
- Java Applications
  (3D games)
  (3D animations)
- Display List
- Texture Data
- Embedded Applications

- Java API
- Graphics Driver/Library
- Real Time Monitor

HW
- Hardware
D504i Demo(Racing)
D504i Demo(Dancing)
Conclusions

• First attempt to implement 3D graphics accelerator on mobile phone
• Small LSI core \((11\text{mm}^2\text{ for logic circuit})\)
• Low power consumption \(38\text{mW}\)
• Low clock frequency \(30\text{ MHz}\)
• Real time acceleration of more than 7fps
• High geometry processing performance
• Geometry engine executes skinning and key frame animation
• Java API and applications can be downloaded from network
Future Work

• Higher performance
  – Parallel processing
  – High clock frequency and Low voltage
  – High resolution screen

• Low power consumption
  – Fine grained gated clock control

• Small core size
  – Cache architecture

• NPR
## Current Status

<table>
<thead>
<tr>
<th>Version</th>
<th>Improvements</th>
<th>Status</th>
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<tbody>
<tr>
<td>Z3D-1</td>
<td>First version</td>
<td>Shipping (5/2002)</td>
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<tr>
<td></td>
<td>First pixel performance</td>
<td></td>
</tr>
<tr>
<td>Z3D-3</td>
<td>Cache architecture</td>
<td>Development has done</td>
</tr>
<tr>
<td>Z3D-4</td>
<td>???</td>
<td>planning</td>
</tr>
</tbody>
</table>
D505i

- New mobile phone implementing Z3D-2
D505i Demo
Thanks

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