GI-Cube: An Architecture for Volumetric Global Illumination and Rendering

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Outline

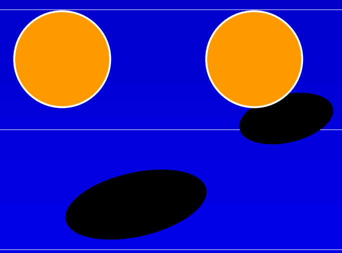
- ➢ Introduction
- Related Work
- Algorithms
- Hardware
- Simulation
- Results & Discussion
- Conclusion

Introduction

- Volume rendering hardware
- Parallel ray tracing
- Parallel radiosity
- Scalable
- Static object - based partition
- Ray reordering
- Flexible ray processing

Introduction

- Single PCI board
  - DSP interface
  - Single - chip pipelined ASIC
  - Rambus DRAM
  - eDRAM



- Global illumination
  - Lifelike rendering improves understanding
  - Reflections, shadows, indirect illumination
    - Clarify spatial relationships

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Related Work

- Volume rendering hardware
  - General purpose [Cabral et al. 94]
  - Special purpose [de Boer et al. 96] [Meissner et al. 98] [Pfister Kaufman 96]
  - Multithreading [Vetterman et al. 99]
  - Commercially available [Pfister et al. 99]
- Global illumination
  - Perception [Levoy et al. 90]
  - Coherence, reordering [Pharr et al 97]

Related Work

- **Global illumination**
  - **Volumetric shadowing**
    [Kajiya von Herzen 84] [Meinzer et al. 91]
    [Sobierajski Kaufman 94]
    [Behrens Ratering 98]
  - **Transport theory**
    [Krueger 91]
  - **Participating media**
    [Pattanaik Mudur 93] [Sillion Puech 94]
    [Perez et al. 97]

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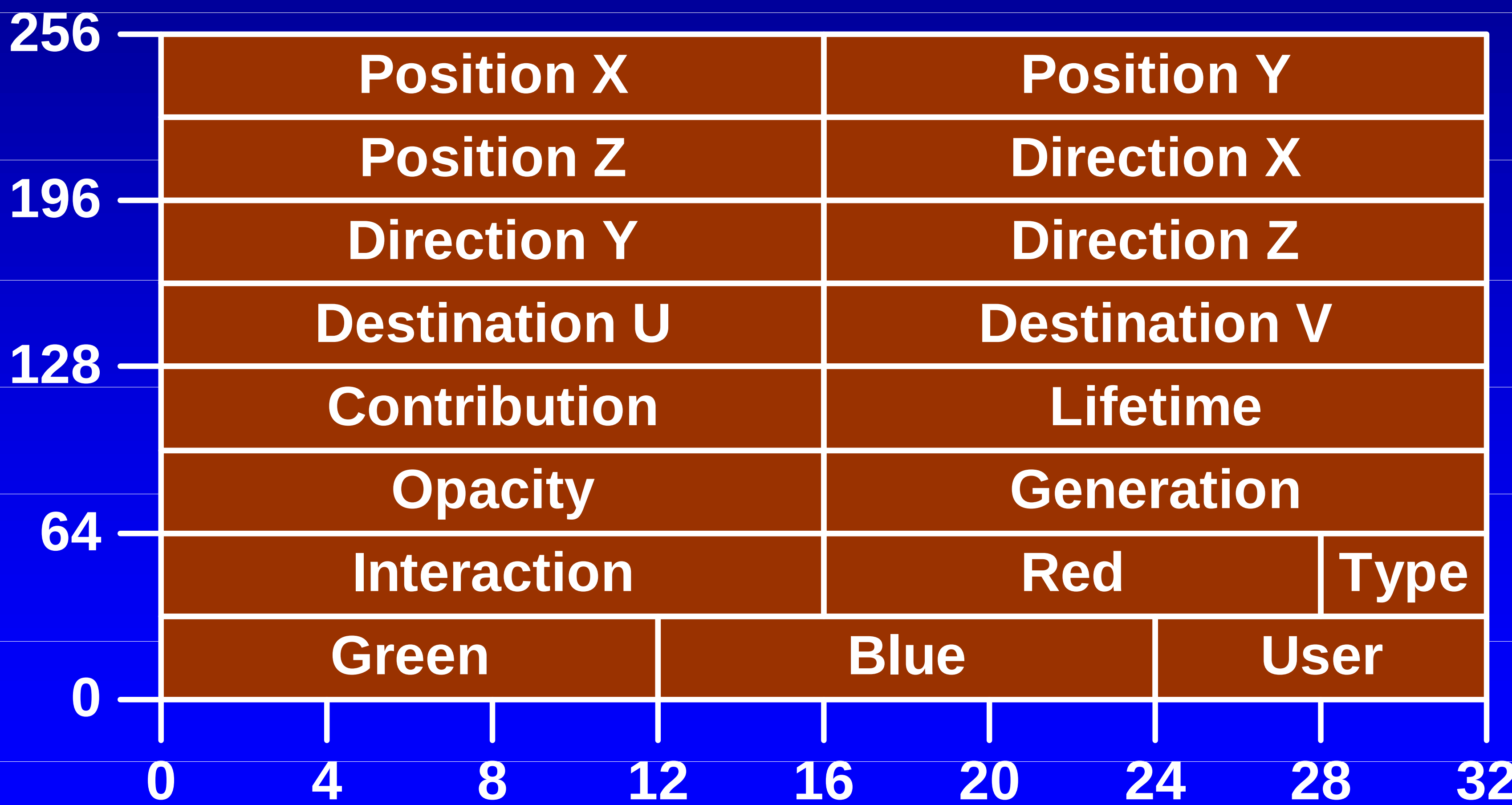
Algorithms

- A cache – conscious volume ray tracing coprocessor
- Accelerates
  - Direct volume rendering
  - Globally illuminated volume rendering
  - Generalized ray tracing, e.g.,
    - Hyper – texture
    - Photon maps
    - Tomographic reconstruction
    - BSDF evaluation

Algorithms

- Ray packet – 256 bits

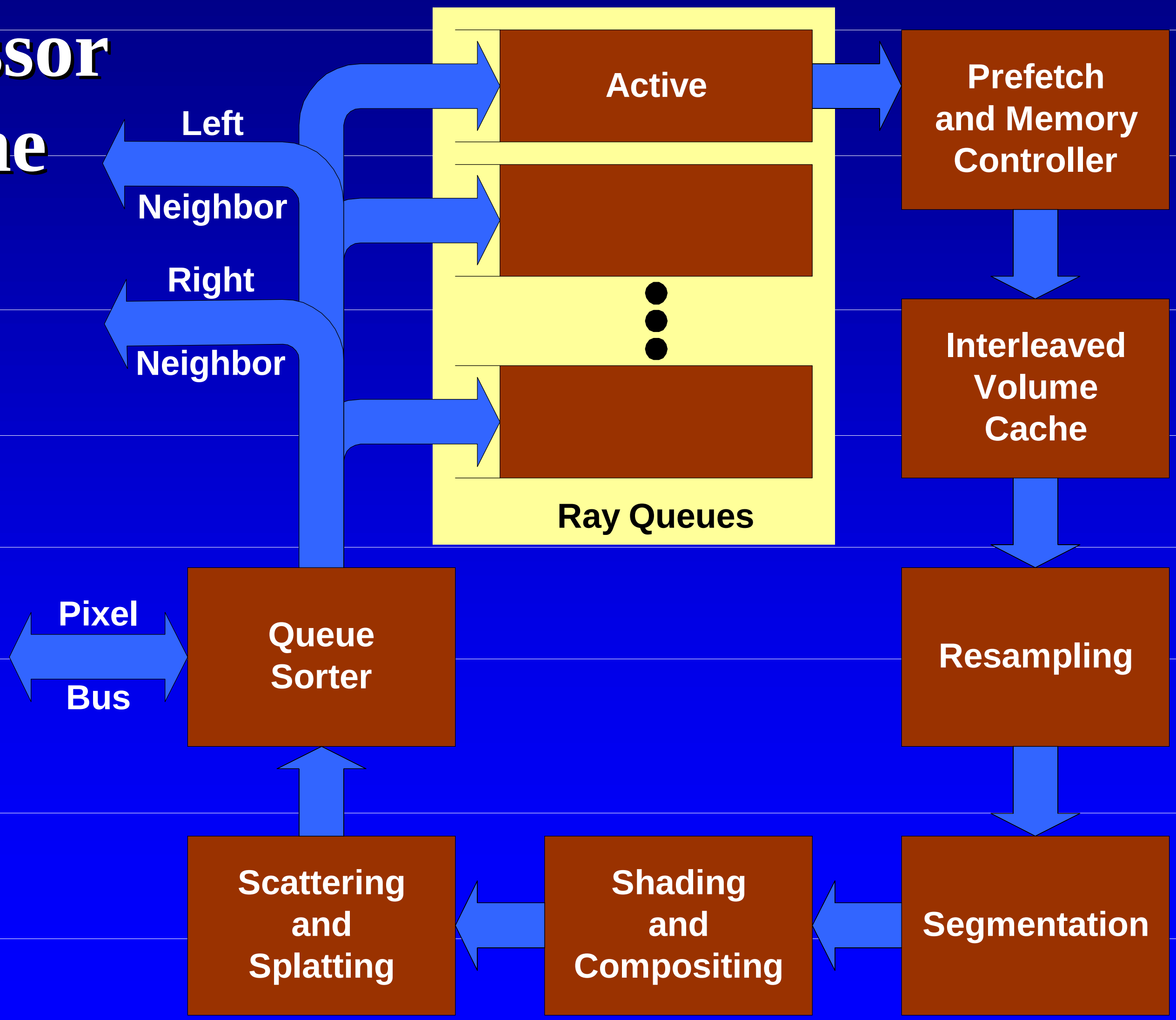


Algorithms

- Base configuration
  - 256^3 volume, 32^3 blocks, 4 processors
- Hybrid image – object order
  - Rays queued on blocks
  - Blocks processed sequentially on processor
  - Rays passed between blocks
- Processor has multiple queues
  - Processes most important queue first
  - Processes round – robin within queue

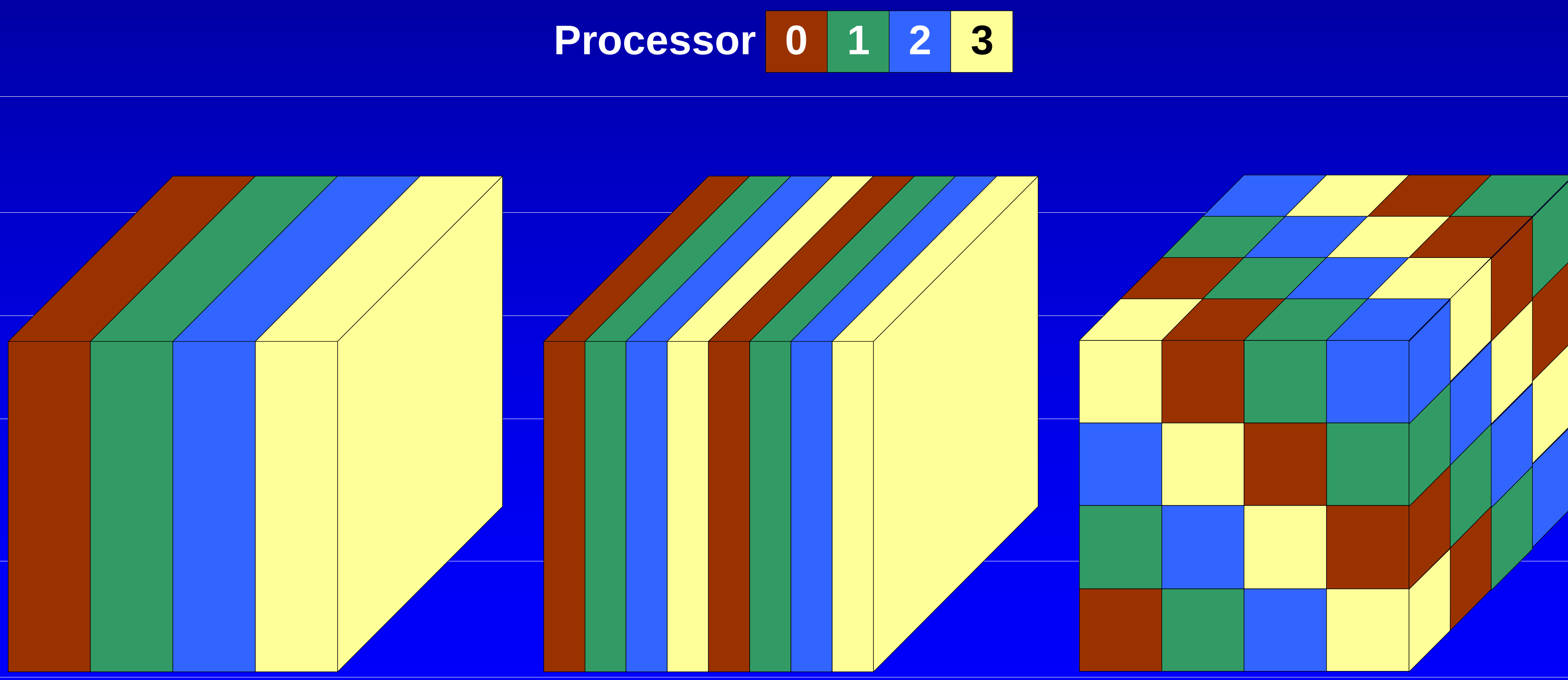
Algorithms

- Processor pipeline



Algorithms

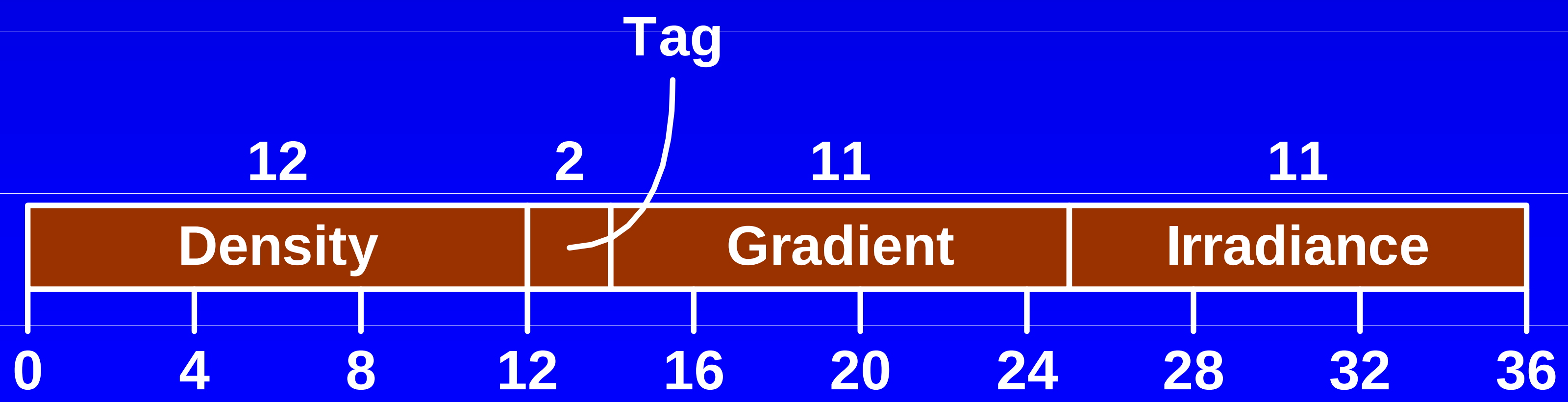
- Parallel partitioning – load balance, communication, & coherence



Simple Slab | Repeating Slab | Block Skewed

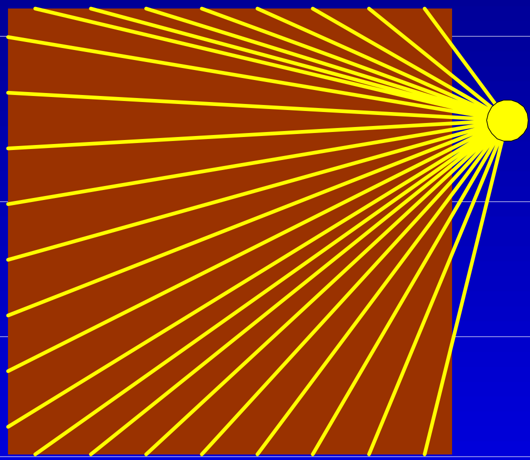
Algorithms

- Global illumination
  - Two – pass, bidirectional
    - Light tracing
    - Ray tracing
  - Generalized rays
  - Splatting

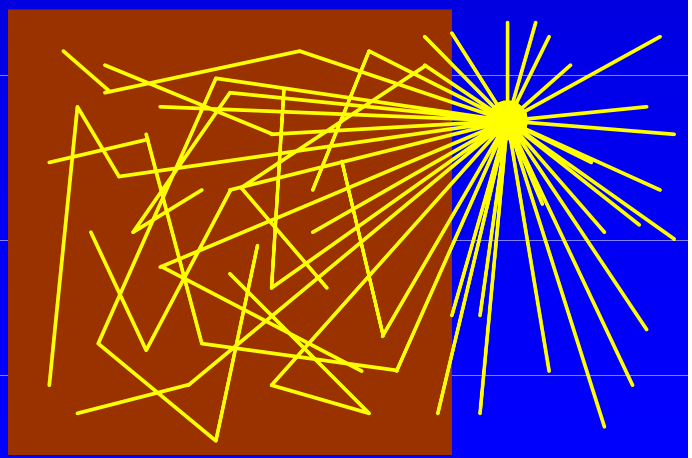


Algorithms

- Global illumination modes
  - Low albedo
    - Few rays, little scattering
    - Good for shadowing
    - Fixed # rays sent to each edge voxel



  - High albedo
    - Many rays, much scattering
    - Good for clouds, radiosity
    - Large # rays sent randomly



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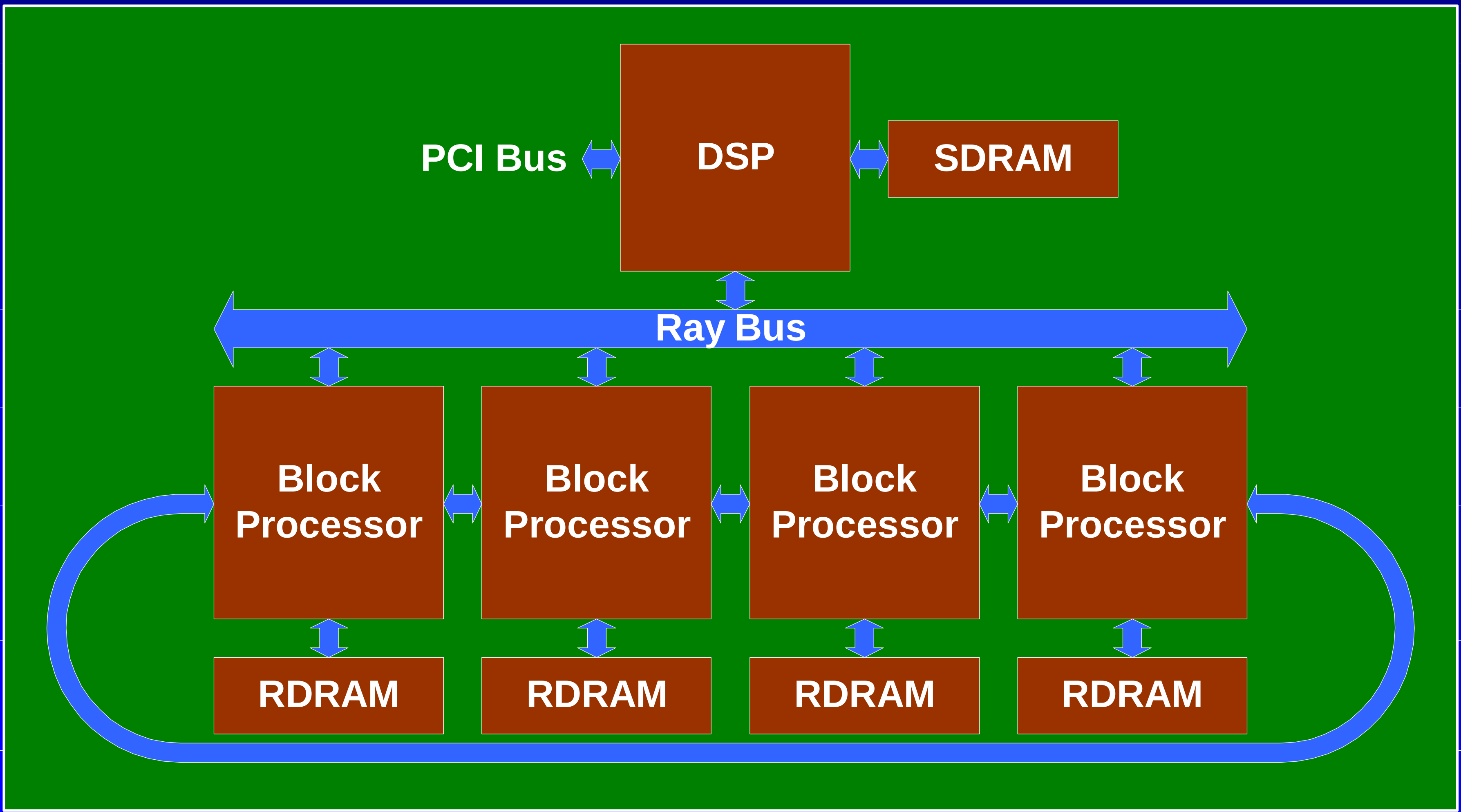
Hardware


PCI Bus
DSP
SDRAM
Ray Bus
Block Processor
Block Processor
Block Processor
Block Processor
RDRAM
RDRAM
RDRAM
RDRAM

Hardware

- Four components
  - DSP, Processors, Memory, and Pipelines
- DSP
  - Interface
  - Controller
  - Loads dataset
  - Generates rays
  - Assembles image
  - Relies on scratch SDRAM

Hardware

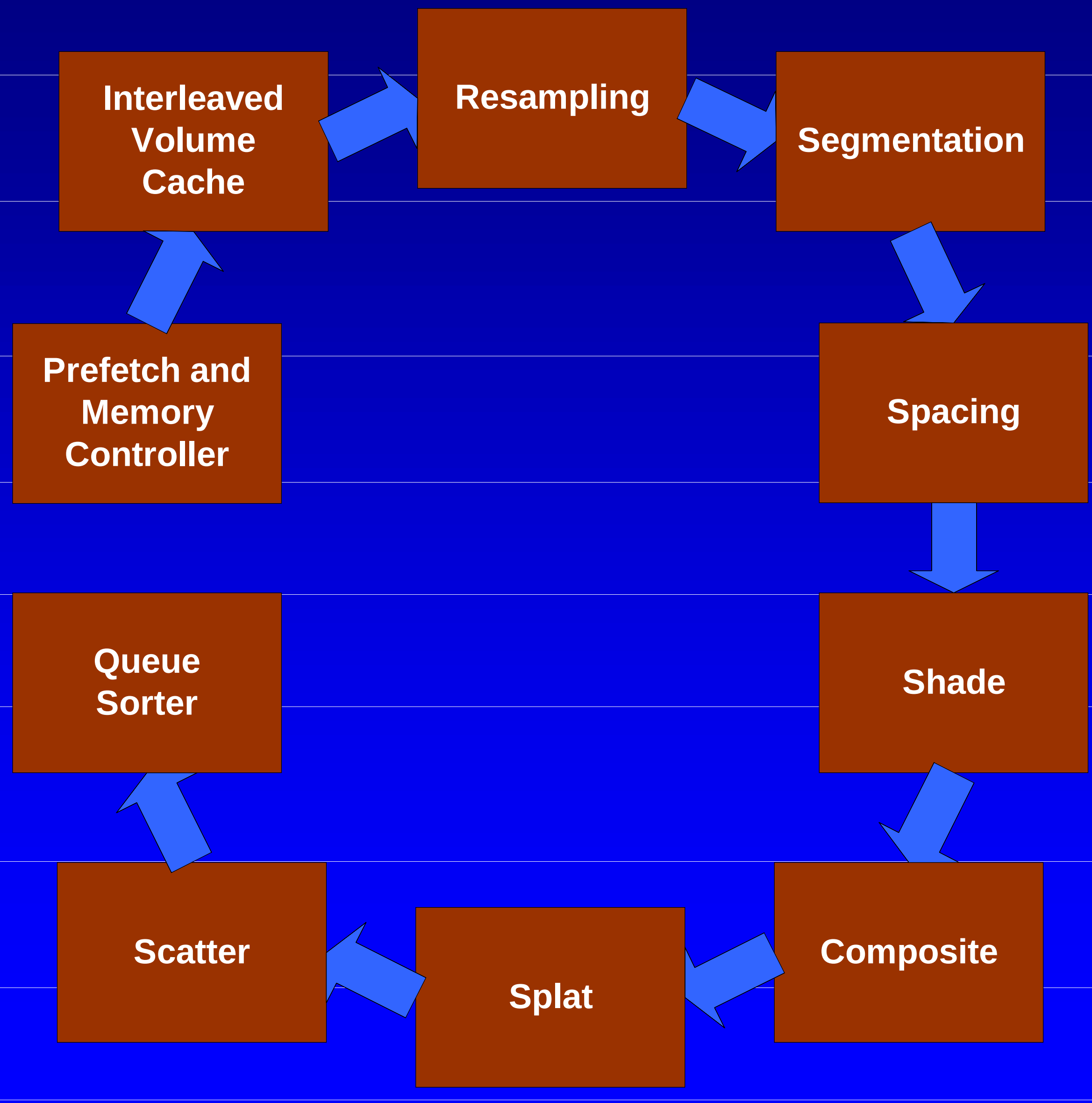
- Processors
  - Take one sample per cycle
    - Barring stalls
  - Maintain and sort queues
    - Pipelined insertion sorter
  - eDRAM for ray queues
    - High on – chip bandwidth
    - Regular access pattern
  - Communication
    - DSP, Neighbors

Hardware

- Memory
  - Parallel, distributed, scalable
  - Static load balance
  - RDRAM for bandwidth
    - 1.6 GB/s available
    - 2.8 – 4.6 GB/s required
    - 18-bits at 800 MHz
    - 4 voxels per 100 MHz pipeline cycle
  - DDR alternative

Hardware

- Pipeline



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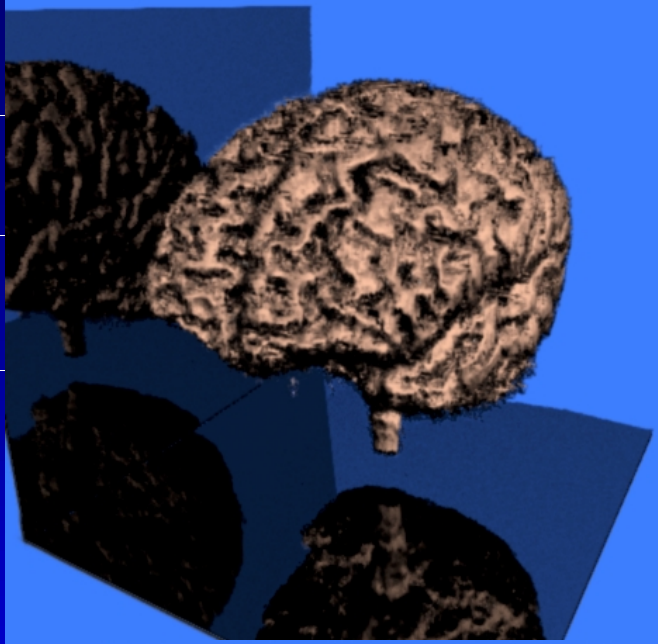
Simulation

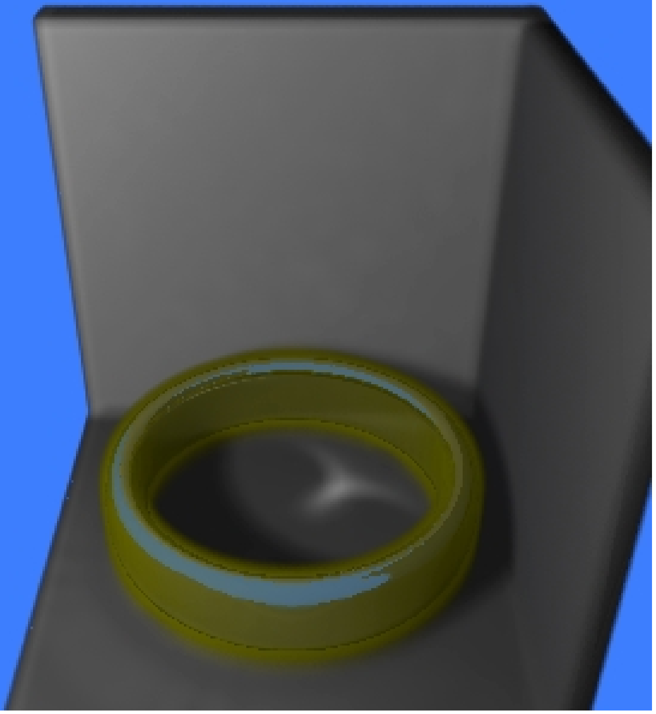
- Two simulators
  - Algorithmic
    - Multi – threaded
    - Flexible
    - Initial testbed
  - Hardware
    - Single – threaded
    - Bit and cycle accurate
    - Gathered exact statistics

Simulation

- Direct volume rendering, reflections
  - 300^2 image, 44 Hz

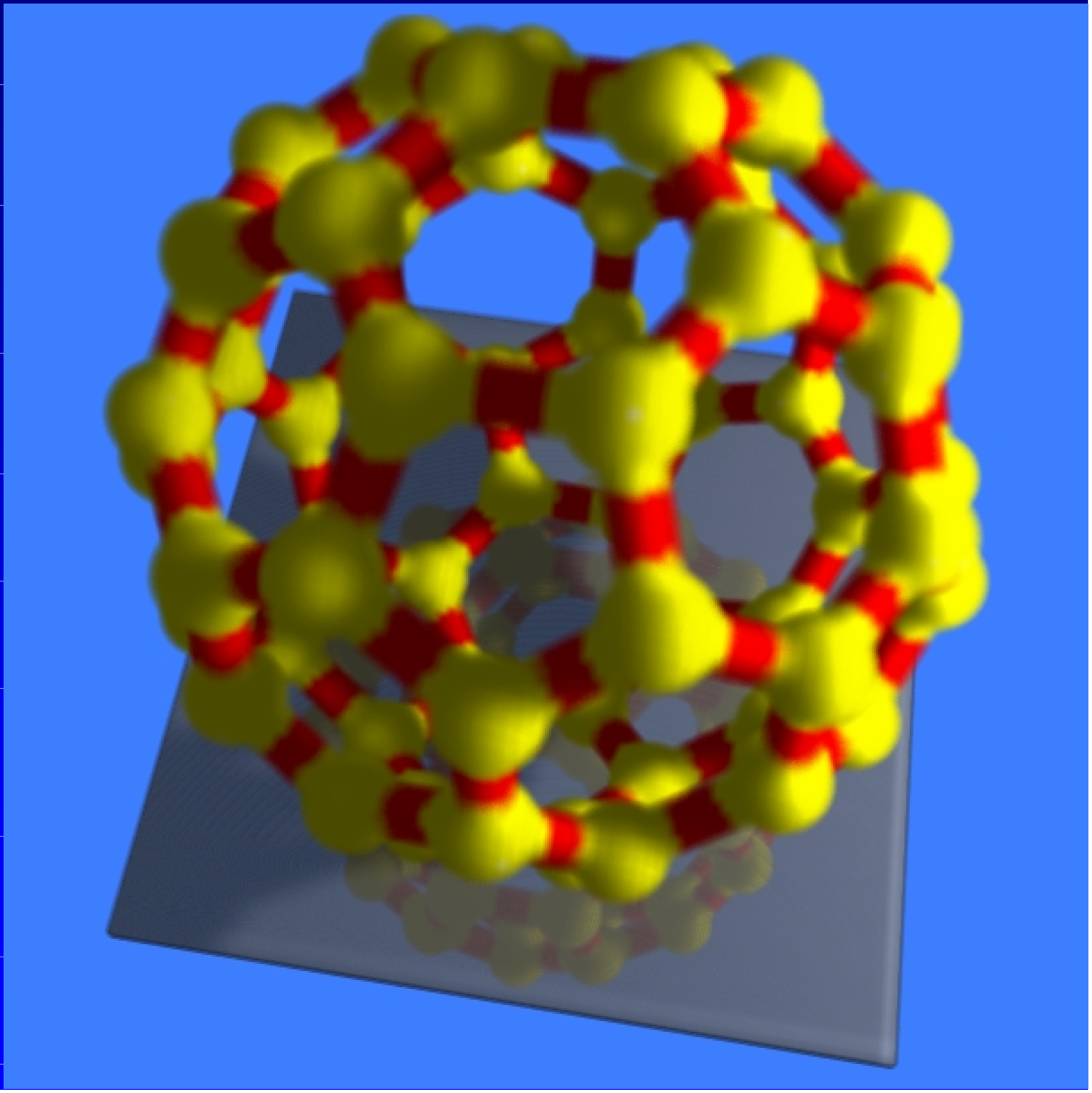


- Caustics (GI)
  - 300^2 image, 2 Hz



Simulation

- C_{60} molecule
  - – Shadows
  - – Reflections
  - – Caustics
  - – Lighting
    - • 361 ms
  - – Rendering
    - • 39 Hz



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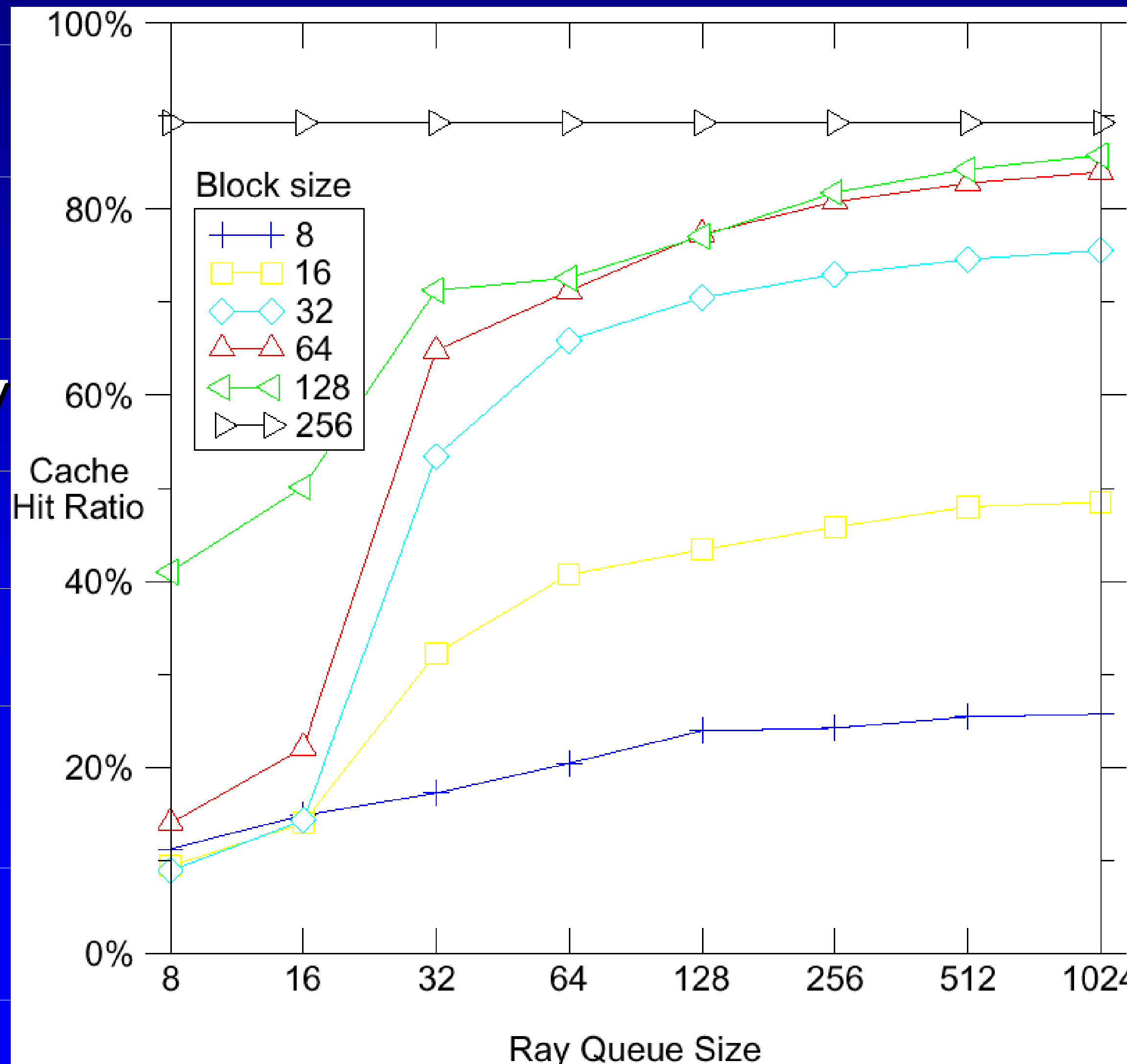
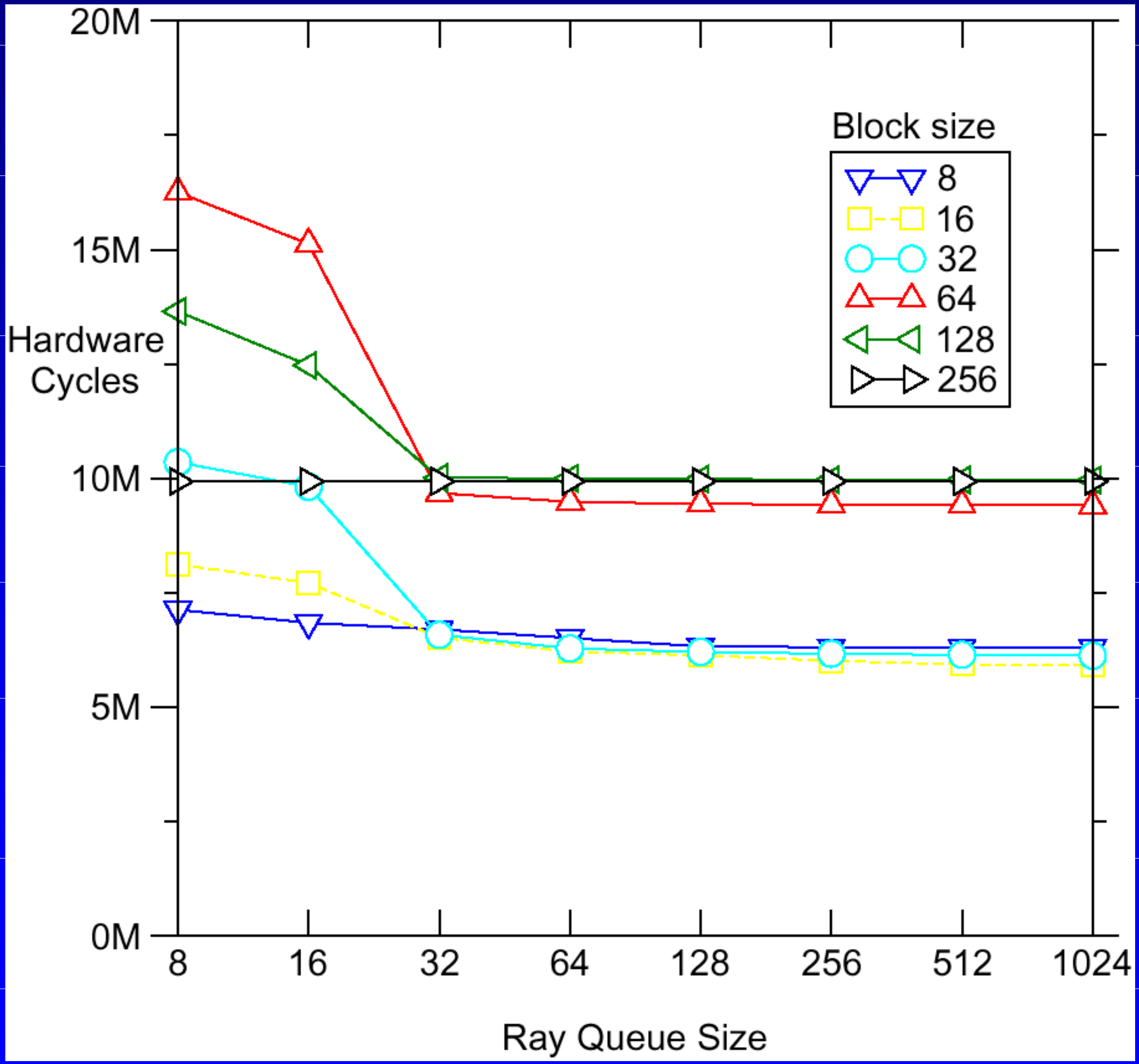
Cache Effectiveness

- Bigger blocks
  - Better
- Compulsory misses
- Pipeline latency
- Design point



Rendering Time

- Smaller blocks
  - Better
- 8×8×8
- Pipeline latency
- Design point



Reordering

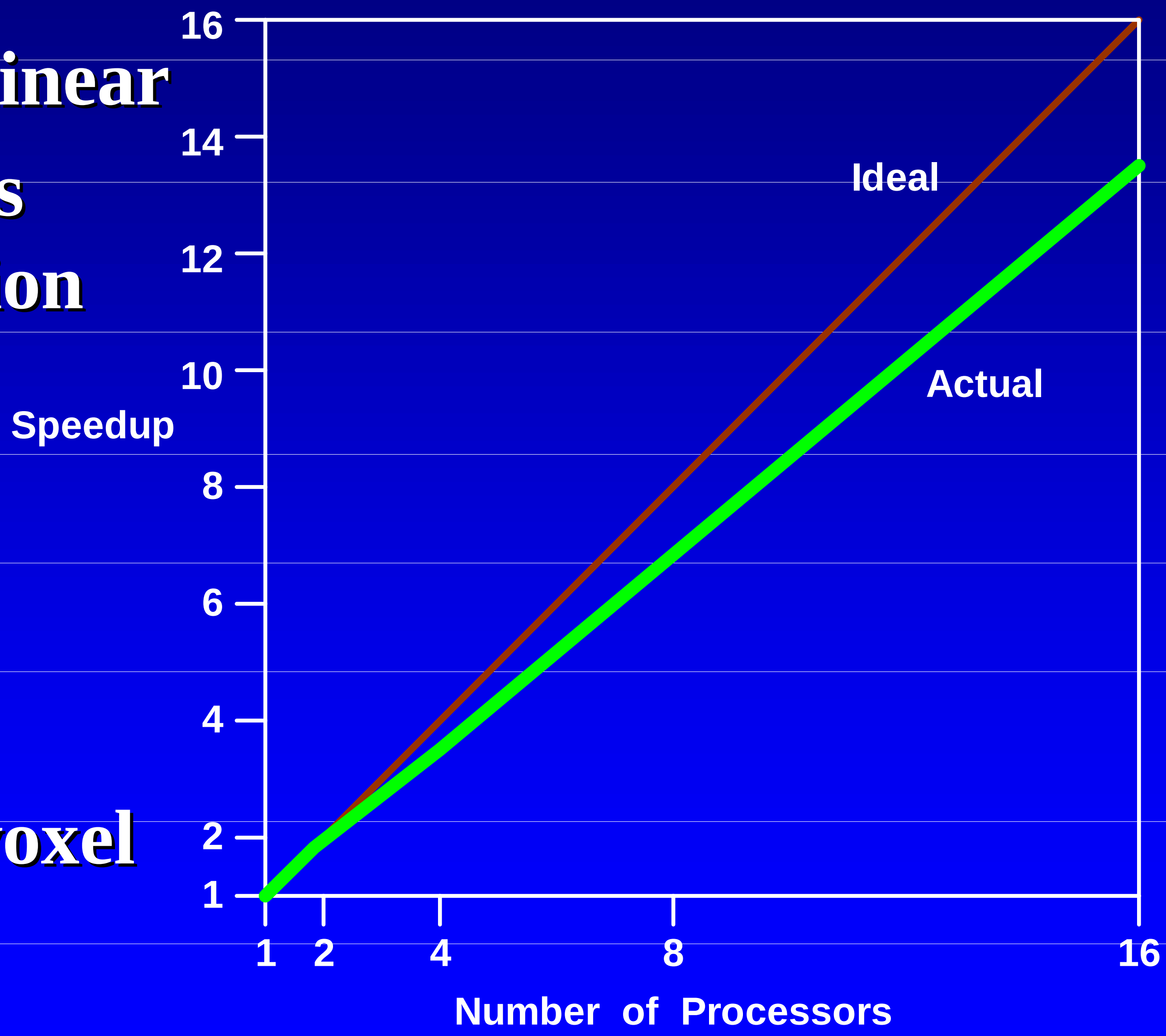
- Evaluate reordering algorithm relative to cached volume rendering

Measure	*Cache*	*Reordering*
Processor throughput	52%	93%
Memory bandwidth	1.9 GB/s	0.8 GB/s
Frame rate	9.2 Hz	16.3 Hz

Scalability

- Near – linear
- Ray bus contention

- Pixel : voxel



Pixel – to – Voxel Ratio

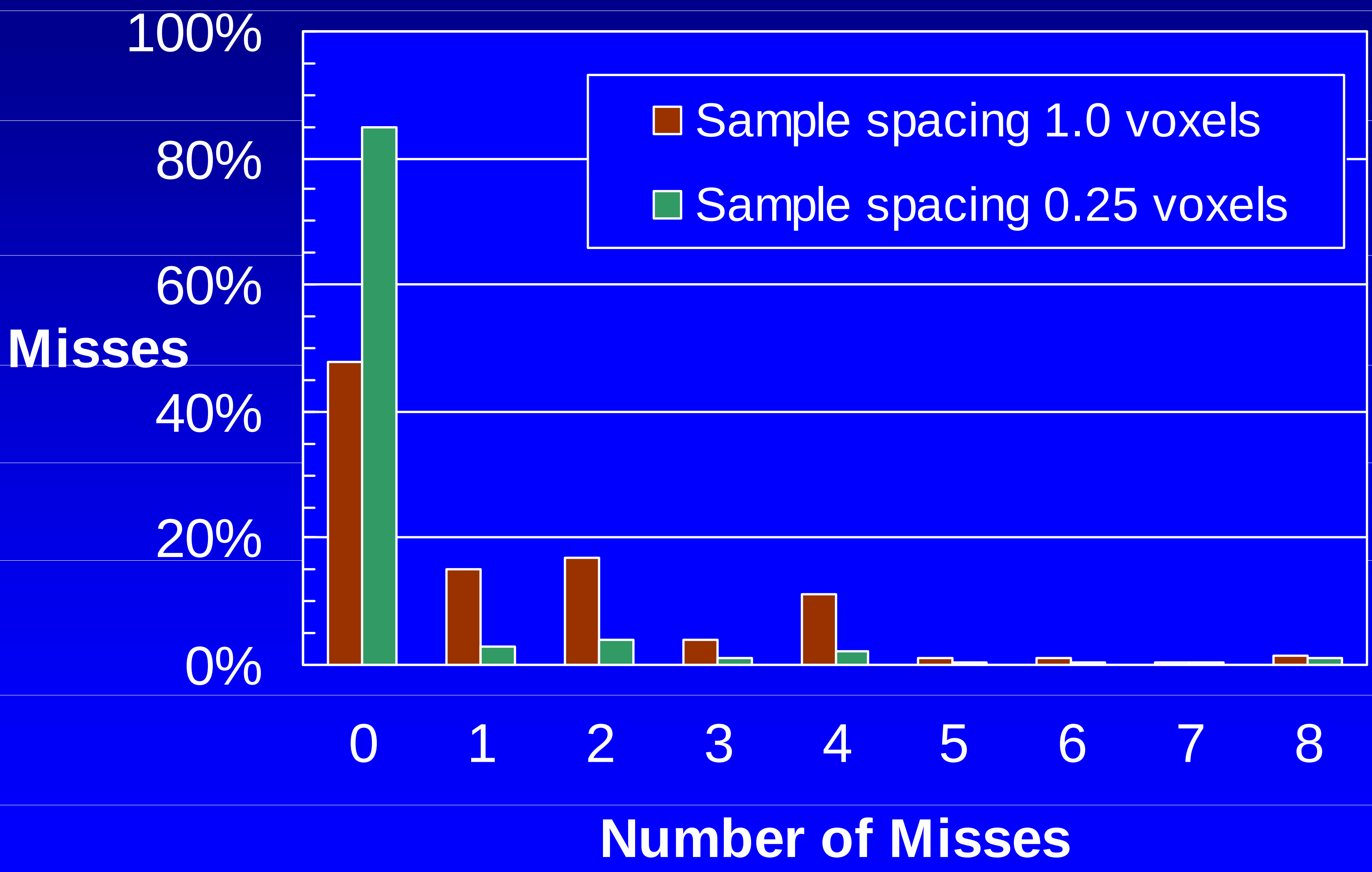
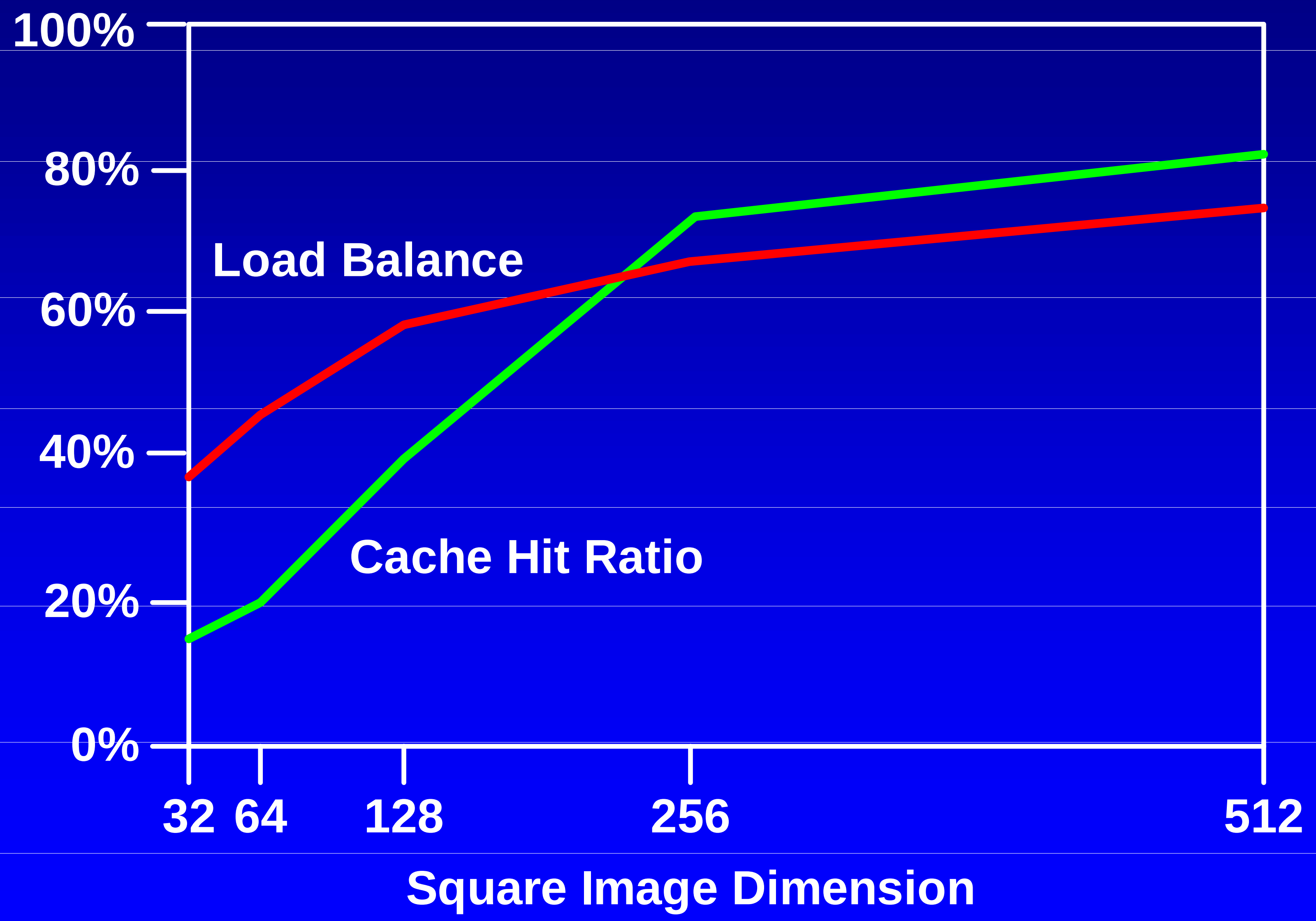


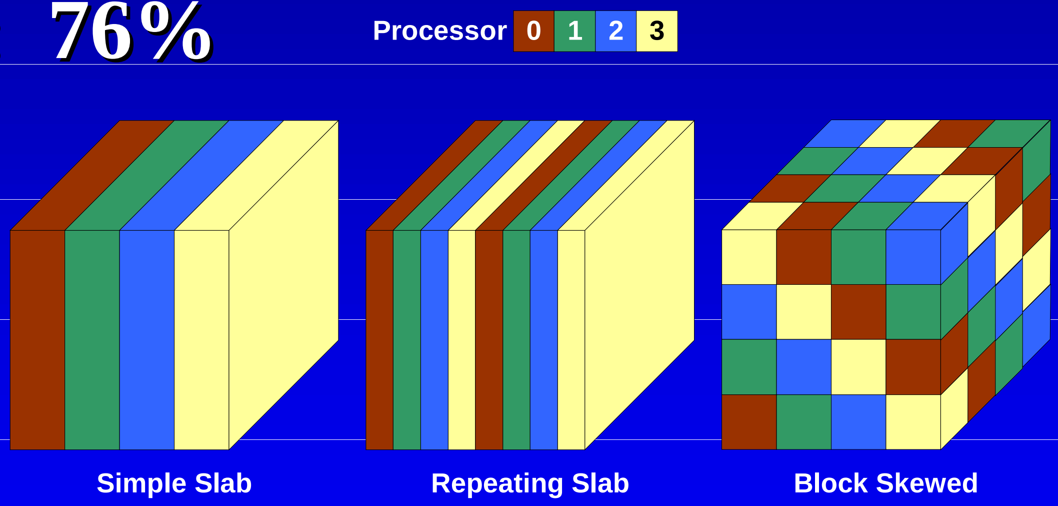
Image Size



100%
80%
60%
40%
20%
0%
Load Balance
Cache Hit Ratio
32
64
128
256
512
Square Image Dimension

Load Balance

- Simple slab: 91%
- Repeated slab: 92%
- Block skewed: 76%



- Block skewed
  - 19% longer
  - Greater communication costs

Algorithmic Enhancements

- Designed into hardware
  - Free
- Data dependent

Improvement	*Minimum*	*Average*	*Maximum*
Space leaping	0%	21%	34%
Early ray termination	0%	12%	24%

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Conclusion

- Flexible, scalable volumetric ray tracing
- Accelerates direct volume rendering
- Supports global illumination
- Extensively simulated
- Reordering doubles frame rate
- Near – linear scalability
- Feasible implementation

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