3D Graphics LSI Core for Mobile Phone "Z3D"

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Abstract

- Architecture of 3D graphics accelerator on mobile phone
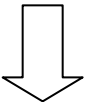

D504i Mobile Phone Mounting Z3D

Outline

- Background
- Development Concept
- System Architecture
- Performance
- Power Consumption
- Conclusions
- Demos

Graphics System Trend

- **Dedicated Machine**
  - Flight Simulator/CAD system using general purpose computer systems
  - Huge system

⇩

- **UNIX workstation**
  - Several boards

⇩

- **PC**
  - PCI/AGP board/LSI Chip

⇩

- **Mobile Phone/Terminal**
  - **Small LSI Core/Low Power Consumption**

Mobile Phone's Display Trend

- **High Quality LCD**
  - Full Color
    - 260K colors, (R,G,B)=(6,6,6) bits
  - Large size
    - 2.1 inches → 2.2 inches
  - High Resolution
    - 132x176 → QVGA(240 x 320)

- **From Wireless Phone to Multi-Media Terminal**
  - Same way PC traced

Contributions

- First attempt to have implemented a graphics accelerator on mobile phone
- Geometry engine architecture
  - At low clock frequency
  - Animation functions except for low level geometry processing
- Rendering pipeline architecture running with low power consumption
- Total system architecture including JAVA-API and content manufacturing

Development Concept

- More than 7fps animation
- Low power consumption
- Low clock frequency
- Small LSI core
- CPU power free
- Open API architecture
  - Easy content development
  - To use commercial modeler

D Graphics Applications

- Character animation
- Game
- Walk through
- 3D icons

Functions

- ## 3D graphics
  - ### Smooth shading
    - Multi-lights (up to 8 lights)
    - Parallel/point/corn lights
    - Specular high light
  - ### Texture mapping
    - Perspective error correction
    - Bilinear interpolation
  - ### Pixel processing
    - Fog
    - Alpha blending
    - Anti-alias line

- ## 2D acceleration

System Architecture

- **Traditional rendering pipeline**
  - Geometry engine/Rendering engine/Pixel engine
- **Geometry engine**
  - CPU power is low
    - CPU has no floating point processing unit and runs at low clock frequency
- **All graphics memories are implemented**
  - Display list buffer
  - Texture memory
  - Frame Buffer (Z buffer, Stencil buffer)
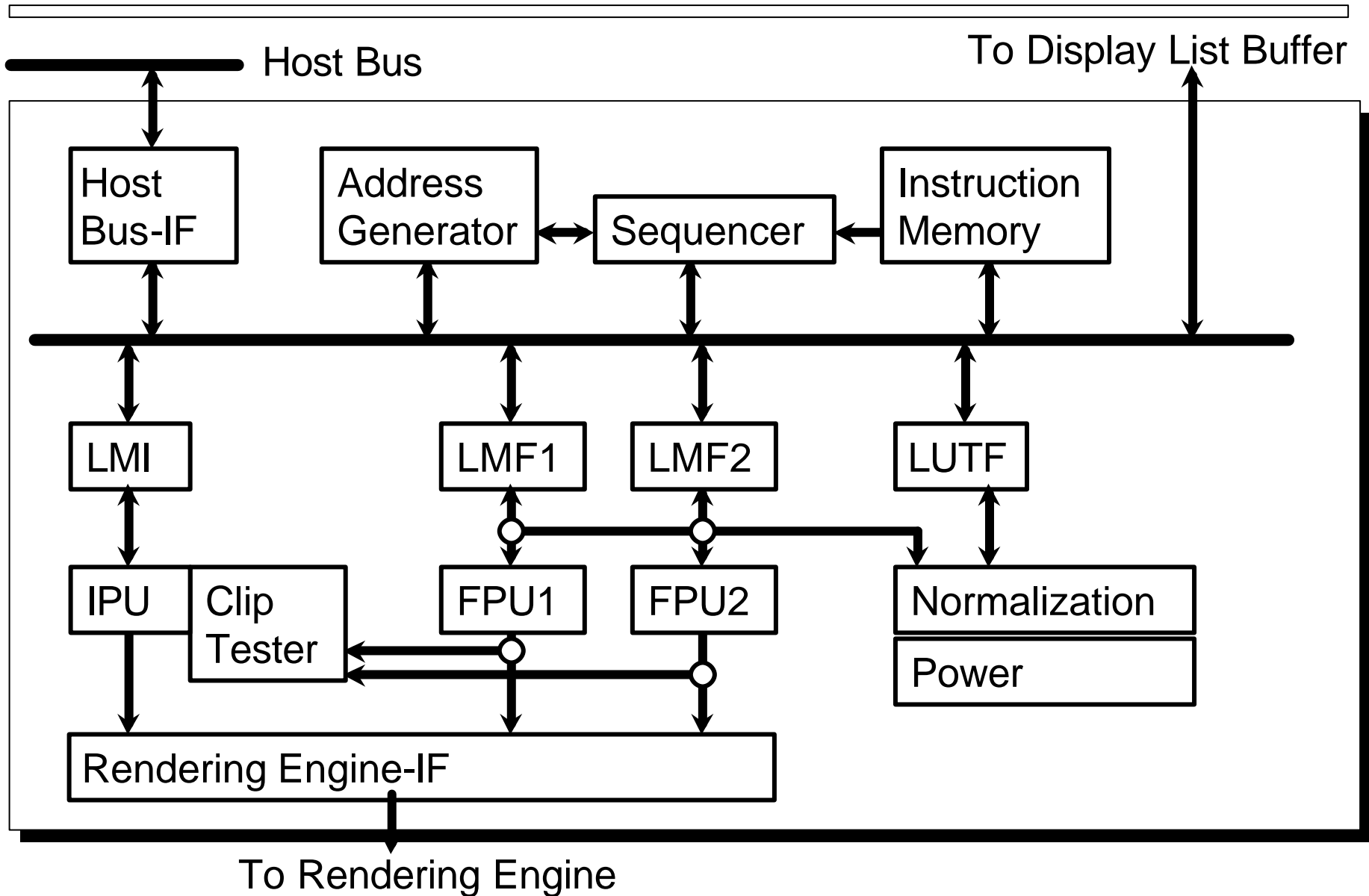- **Gated clock**

Hardware Configuration
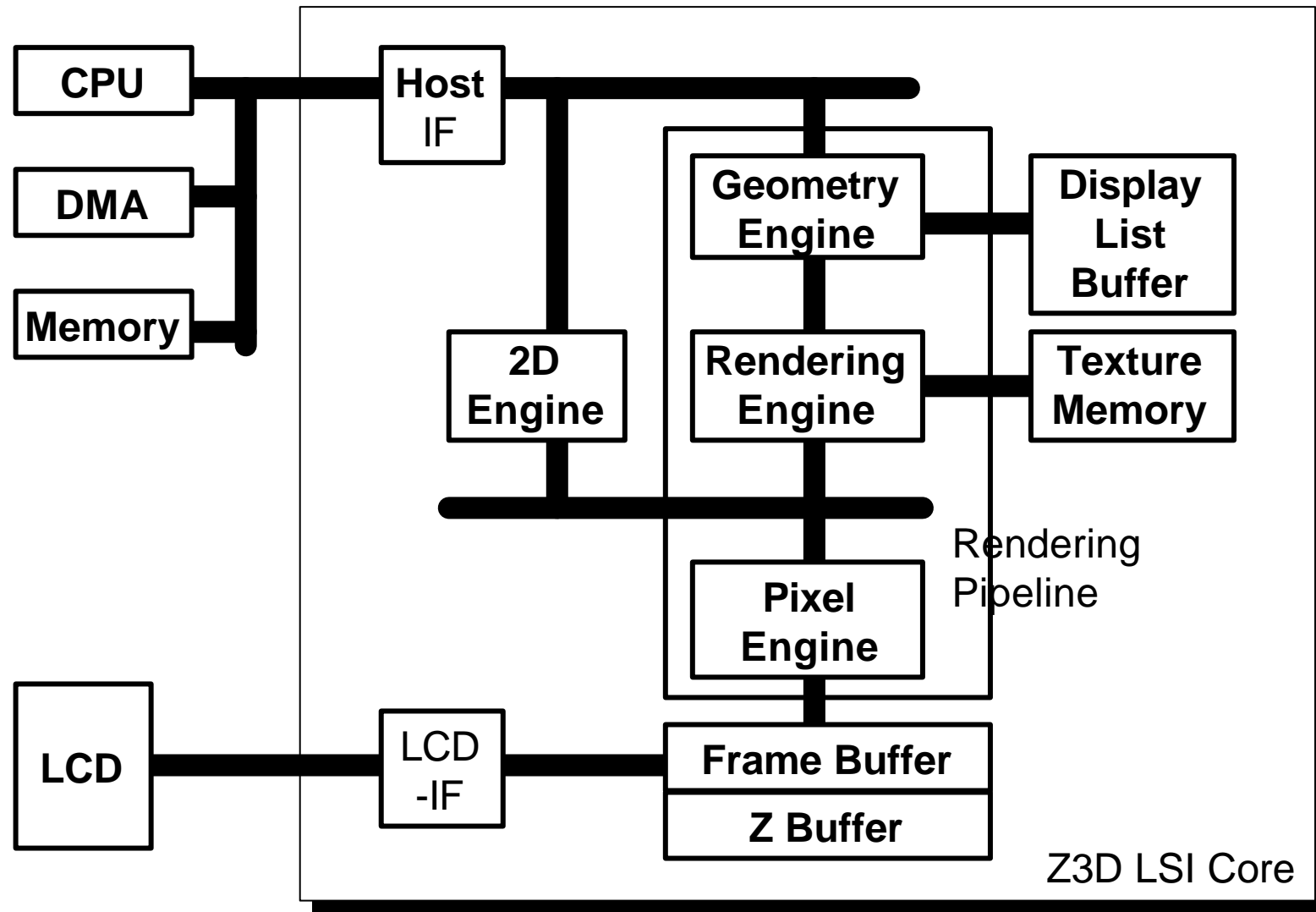
Memories

- Display list buffer
  - 24 bits x 40KW =120 KB

- Texture memory
  - 13 bits x 256 x 128 = 53 KB

- Frame buffer
  - (R,G,B)=(6,6,6)bits, Z = 12bits, Stencil bits = 2bits
  - 32 bits x 132 x 176 = 93 KB

Geometry Engine Architecture

- Micro-code programmable processor like DSP
  - High performance arithmetic processor
  - Manage the data in the display list buffer
- Two parallel SIMD type floating point processor
  - Two 24-bit floating point processing units
    - Because of a small screen
    - 1-bit sign, 7-bit exponent, 16-bit mantissa
  - A 24-bit integer processing unit
- Special floating point processing units
  - Normalization unit (1/(square root(x)))
  - Power unit (x^y)
  - Clip tester

GE Configuration

Host Bus

To Display List Buffer

Host Bus-IF

Address Generator ↔ Sequencer ← Instruction Memory

LMI

LMF1

LMF2

LUTF

IPU | Clip Tester

FPU1

FPU2

Normalization

Power

Rendering Engine-IF

To Rendering Engine

Instruction Pipeline of GE

| Instruction n | F | D | MR | E | WB |

Instruction n | F | D | MR | E | WB |

Instruction (n+1) | F | D | MR | E | WB |

Instruction (n+2) | F | D | MR | E | WB |

→ |1clk| ←

F	: Fetch
D	: Decode
MR	: Memory Read
E	: Execution
WB	: Write Back

GE Micro-code

- ## Geometry processing
  - – Subset of OpenGL
    - • 53 functions (vs. 350 functions of OpenGL)

- ## Animation processing
  - – Key frame animation
    - • Color animation, Location animation, Scalar animation, Rotation animation
    - • Described by VRML
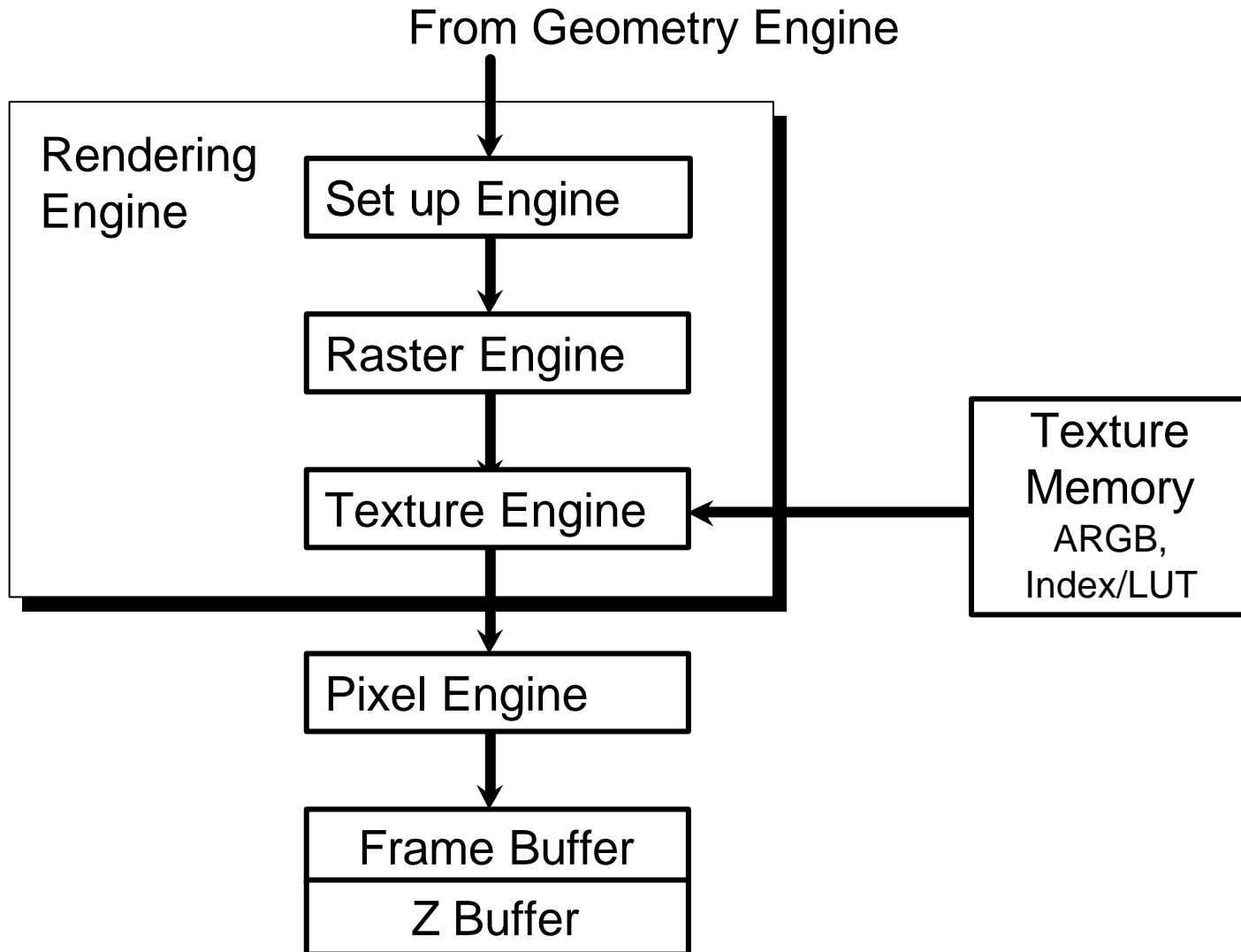   - • Can reduce the data
  - – Skinning

GE Features

- **Compact configuration**
  - 24-bit floating point processing
  - The space of instruction memory and display list buffer are limited
- **Two parallel SIMD type floating point processing**
  - 120Mflops at 30 MHz
- **Special arithmetic processing unit**
  - Normalization, power, clip test
- **Micro-code control**
  - Geometry processing
  - Key frame animation
  - skinning

Rendering Engine/Pixel Engine

From Geometry Engine

Rendering Engine

Set up Engine

Raster Engine

Texture Engine

Texture Memory
ARGB,
Index/LUT

Pixel Engine

Frame Buffer

Z Buffer

Display Sample

- Shading
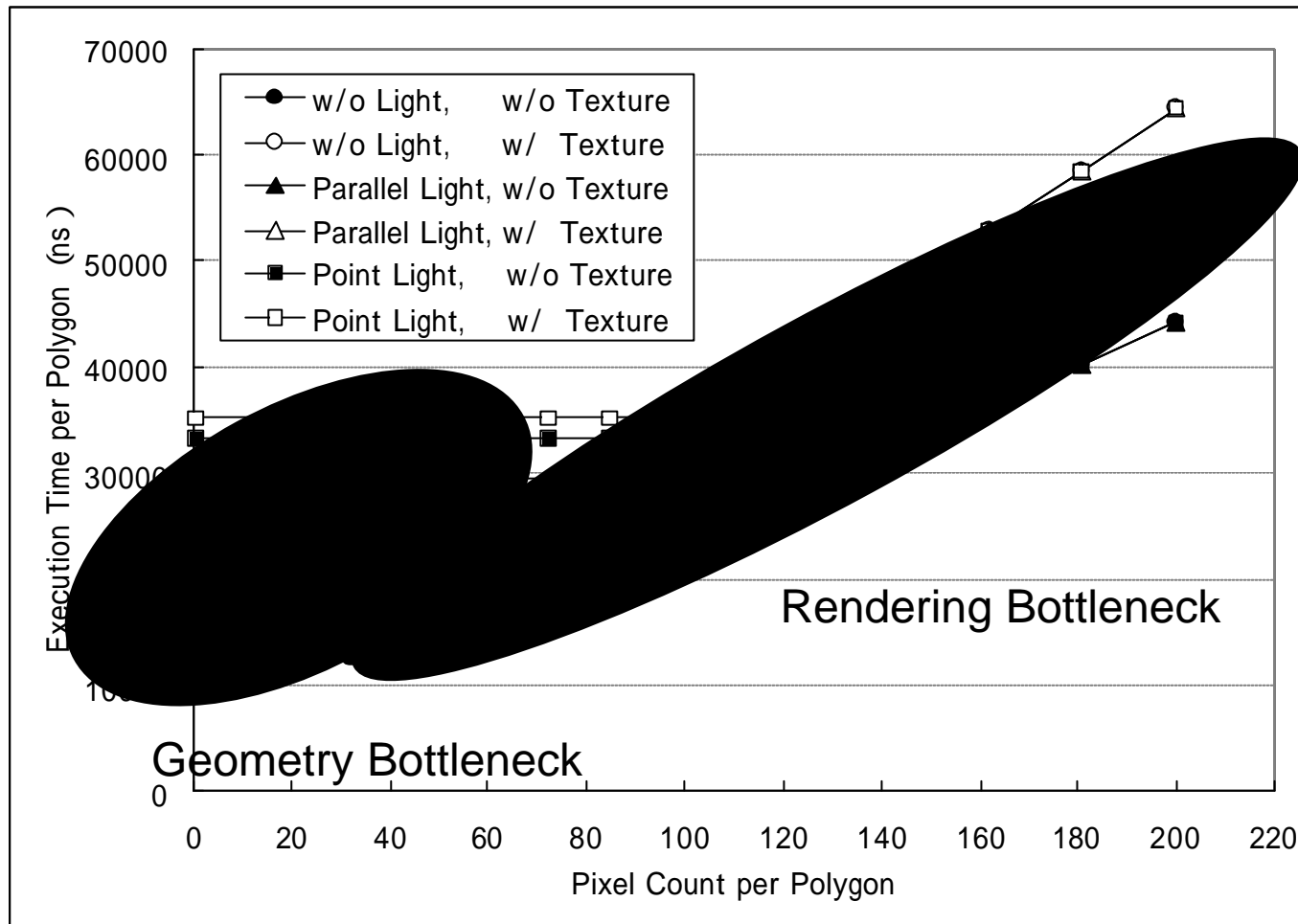- Texture mapping
- Multi lights
- Alpha blending

Performance

- Geometry performance
  - Up to 185Kvertex/sec
- Pixel performance
  - Up to 5Mpixel/sec
- At 30MHz

Actual Performance

Performance curve at pipeline mode, four-vertex triangle strip mode

LSI Implementation

- 360Kgates logic and 2.3Mbits SRAM

- 30 mm^2 using 0.18 um process
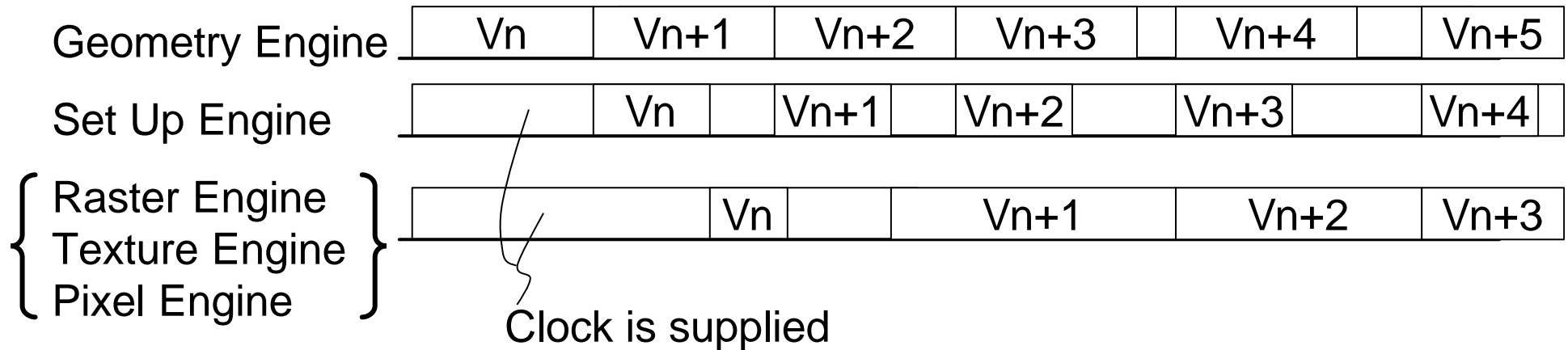 - 11mm^2 for logic
  - 19 mm^2 for SRAM
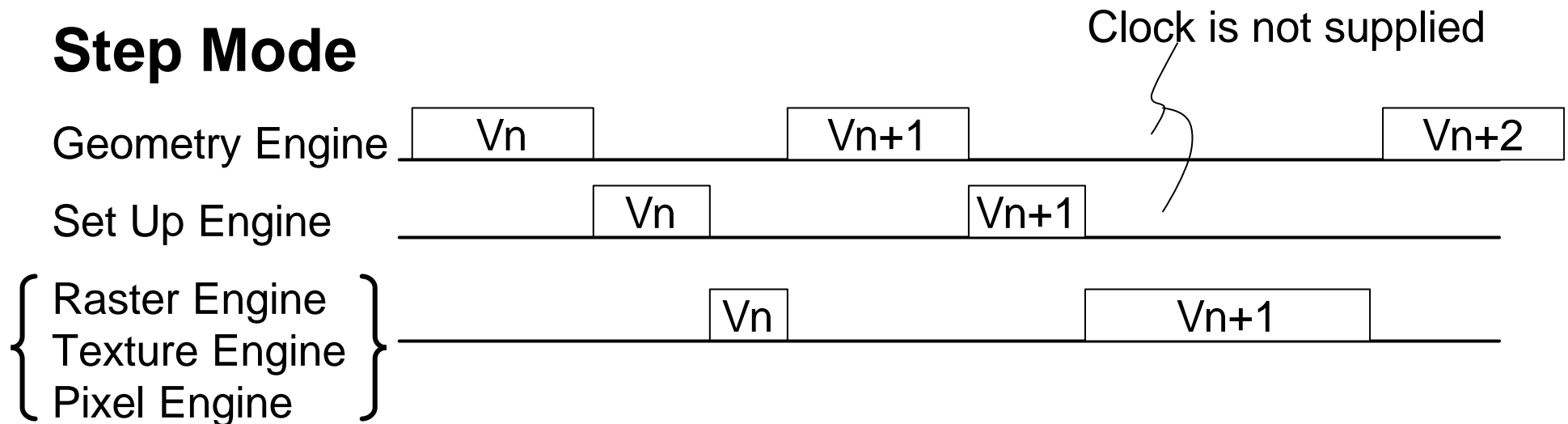
Gated Clock

- General way to reduce power consumption
- Two types
  - Functional block base
    - Clock supply is separated for 3D pipeline, 2D engine and LCD-controller
    - Only one clock is activated
      - When 3D pipeline is working, clocks are not supplied to 2D engine and LCD controller
  - 3D pipeline base (Step mode)
    - Divide 3D pipeline to three portions
      - Geometry engine/set up engine/others(Raster engine, Texture engine, Pixel engine)
      - Clocks are supplied and turned off sequentially and automatically
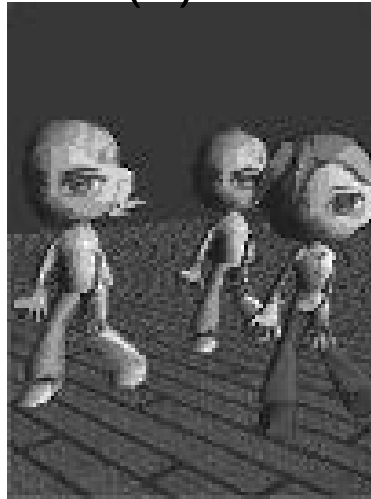
Pipeline Mode vs. Step Mode

Pipeline Mode

Geometry Engine	Vn	Vn+1	Vn+2	Vn+3		Vn+4		Vn+5

Set Up Engine			Vn		Vn+1	Vn+2	Vn+3		Vn+4	

Raster Engine
Texture Engine
Pixel Engine

			Vn		Vn+1	Vn+2	Vn+3

Clock is supplied

Clock is not supplied

Step Mode

Geometry Engine	Vn		Vn+1			Vn+2

Set Up Engine		Vn		Vn+1		

Raster Engine
Texture Engine
Pixel Engine

		Vn		Vn+1	

Power Consumption

Sample Applications

(a)   (b)

Application	(a)	(b)
Vertex count	4690	1717
Polygon count	2134	973
Average pixel count per polygon	6.3	49.8

	Power Consumption		Performance	
	(a)	(b)	(a)	(b)
Pipeline mode	66 mW	66 mW	8.5 fps	19.1 fps
Step mode	38 mW	38 mW	8.0 fps	17.3 fps

Study of Power Consumption

- Content designers like "1 light with texture" mode
  - Geometry performance is bottleneck
    - 80 Kvertex/sec

Geometry Engine	Vn		Vn+1		Vn+2

Set Up Engine — Vn / Vn+1

Raster Engine / Texture Engine / Pixel Engine — Vn / Vn+1
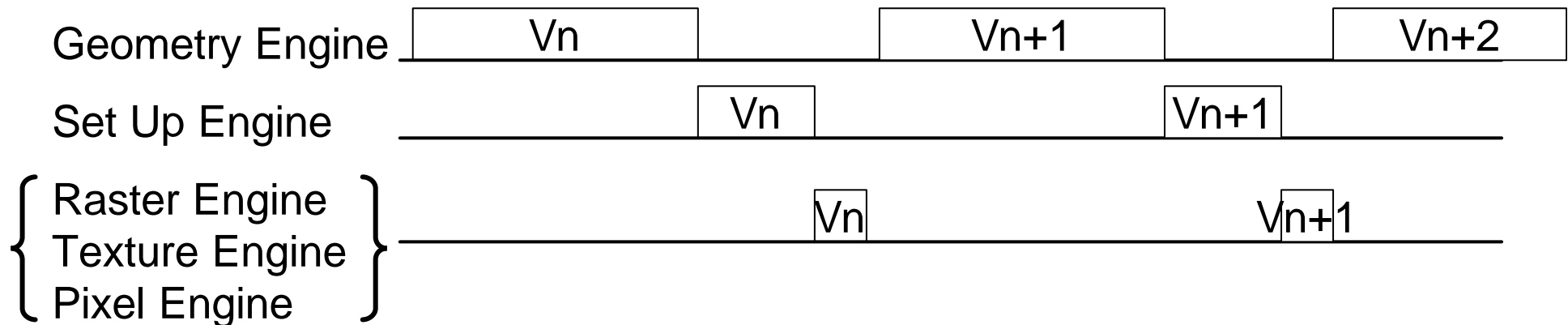
- Power consumption was reduced 43%
- Performance reduction was 6% in application (a) and 10% in application (b)

Software Configuration

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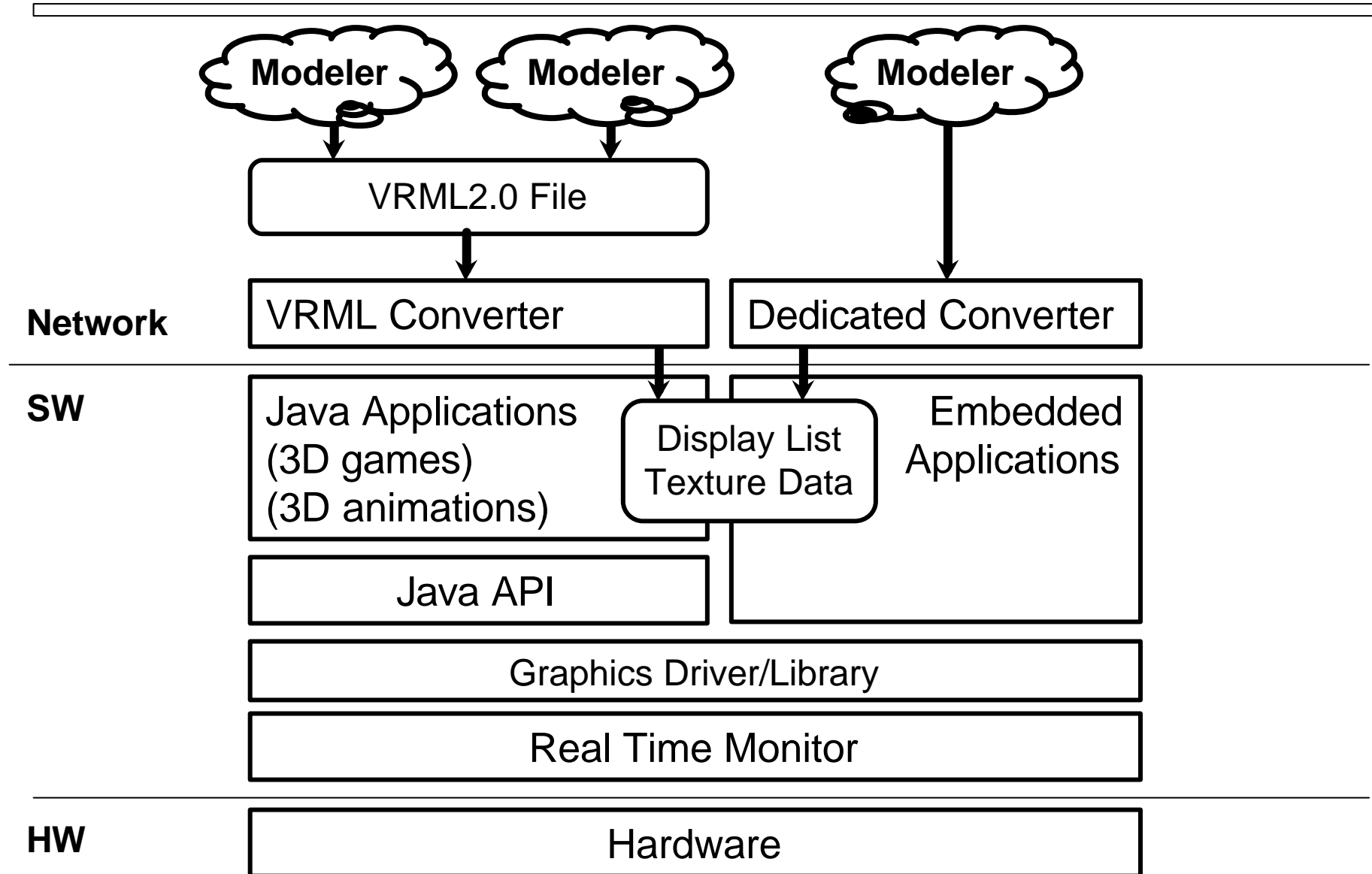
D504i Demo(Racing)

D504i Demo(Dancing)

Conclusions

- First attempt to implement 3D graphics accelerator on mobile phone
- Small LSI core (11mm^2 for logic circuit)
- Low power consumption (38mW)
- Low clock frequency (30 MHz)
- Real time acceleration of more than 7fps
- High geometry processing performance
- Geometry engine executes skinning and key frame animation
- Java API and applications can be downloaded from network

Future Work

- **Higher performance**
  - Parallel processing
  - High clock frequency and Low voltage
  - High resolution screen

- **Low power consumption**
  - Fine grained gated clock control

- **Small core size**
  - Cache architecture

- **NPR**

Current Status

Version	Improvements	Status
Z3D-1	First version	Shipping(5/2002)
Z3D-2	High Resolution(QVGA) First pixel performance	Shipping(5/2003)
Z3D-3	Cache architecture	Development has done
Z3D-4	???	planning

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- New mobile phone implementing Z3D-2

D505i Demo

Thanks

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