A Low-Cost Memory Architecture For PCI-Based Interactive Ray Casting

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Outline

Introduction

- ***GOAL : Interactive Volume Rendering***
  - High quality images
  - Modest costs (PC-Based)
  - Flexible sampling rate
  - Color
  - Parallel and Perspective projections

Introduction

VIZARD I:

- G. Knittel 1997
- Advantages
  - *Up to 7 f/s for 256^3 datasets*
  - *Stereo and parallel projection*
  - *Cheap and portable*
- Disadvantages
  - *Lossy Compression*
  - *Pre-shading and Pre-classification*

Introduction

VIZARD II:

- Independent ray casting accelerator
- Complete rendering pipeline on board
- Parallel and perspective projection
- Cut planes and interactive classification support
- Interactive frame-rates for 256^3 voxels
- Input: Viewing Parameters
- Output: Images

Memory Performance

Why improve Memory Performance ?

- The user wants it faster and bigger
- Frame rate is dominated by memory access time
- Higher speed and storage for larger datasets - 512^3
- Improve caching - VIZARD I - Ray coherence cache

Introduction

Sub-Cubes - Cubic Addressing

- Lichtermann95 - Sub-Cubes
- de Boer96 - Sub-Cubes
- Osborne97 EM-Cube, Block Skewed Memory
- Vettermann99, 8 Parallel Memories with Cubic Addressing

Outline

Introduction

Memory Interface

PCI-Board

Results

Conclusion

Memory Interface

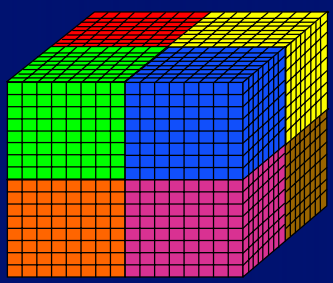
Issues

- 8 voxel neighbourhood for tri-linear interpolation
- Random access
- Modern memories
  - *RDRAM*
  - *SDRAM, Random column read per cycle within page of same bank - Cache*

Memory Interface

SDRAM

1 cache
1 Memory
512 voxels



8 voxels
8 Memories

1 cache
8 Memories
4096 voxels

8 caches
8 Memories

Memory Interface

Organisation

- 8 Memories to read 8 voxel neighbourhood in one cycle
- Addressing calculation based on sub-cubes (8^3)
  - *Cubic Address = Sub-Cube + Voxel Address*
  - *= {x,y,z}/8 + {x,y,z} mod 8*

Memory Structures

64 Memories

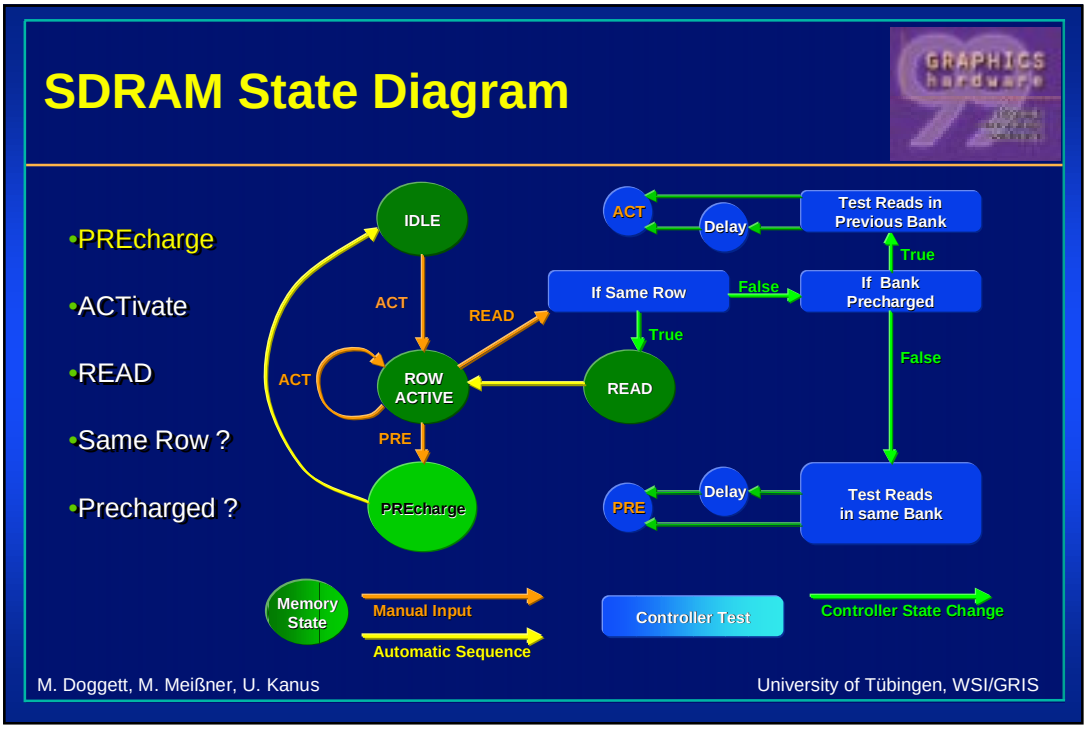
- Maintain 8 active caches
- Activate all 56 neighbouring caches
- Impractical

8 Parallel Memories

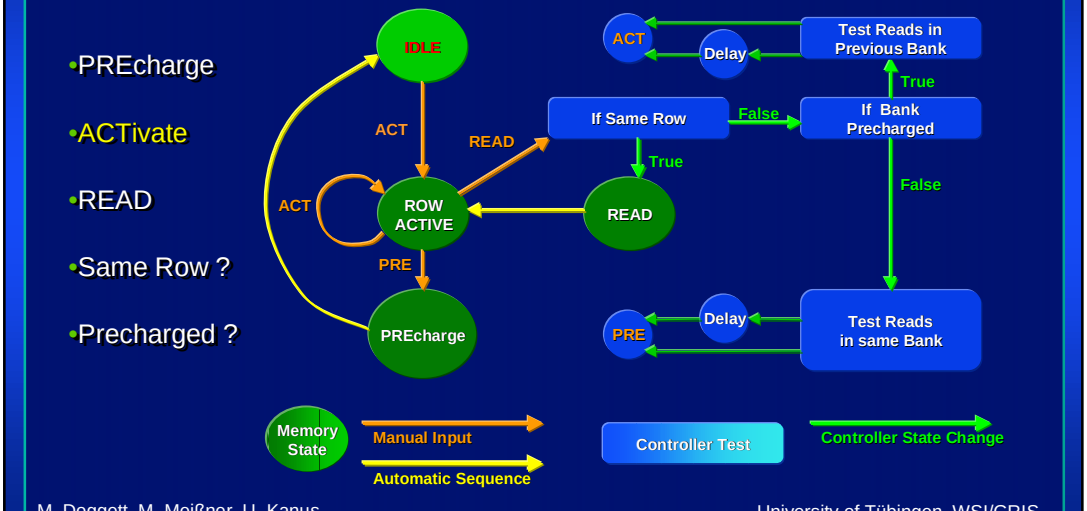
- Feasible
- Stalls at boundaries for row activate and precharge

Prefetching

SDRAM State Diagram



SDRAM State Diagram



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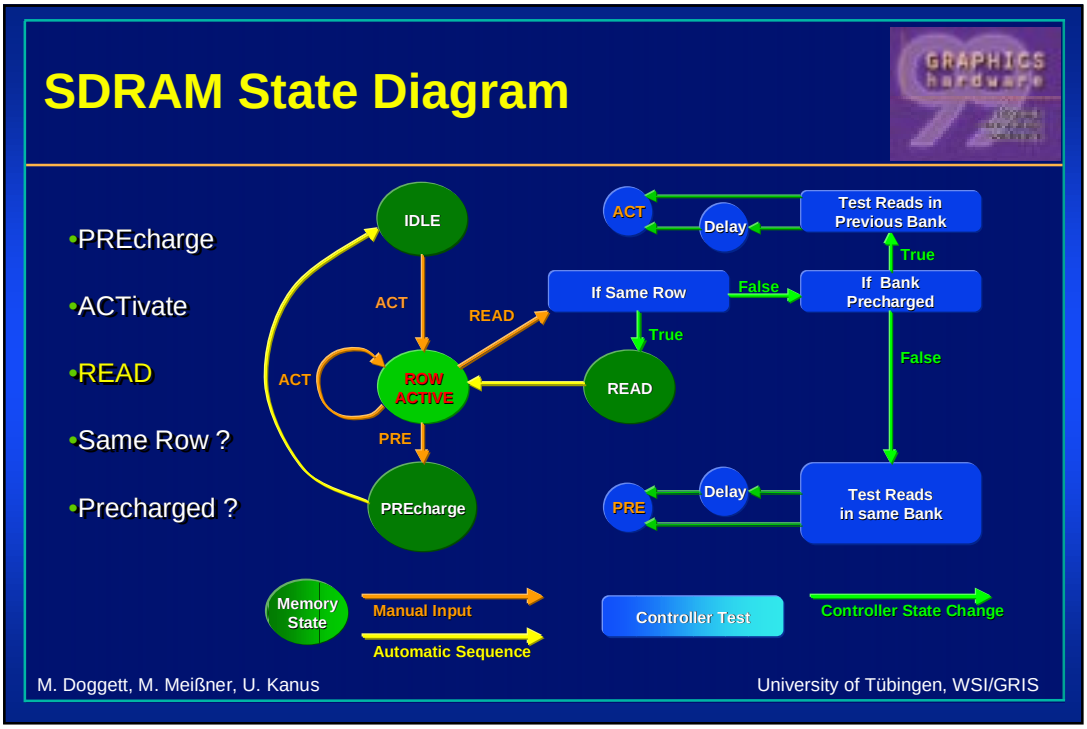
SDRAM State Diagram
GRAPHICS hardware
•PREcharge
•ACTivate
•READ
•Same Row ?
•Precharged ?
IDLE
ACT
READ
ACT
ROW ACTIVE
PRE
PREcharge
If Same Row
False
True
READ
If Bank Precharged
True
False
ACT
Delay
Test Reads in Previous Bank
PRE
Delay
Test Reads in same Bank
Memory State
Manual Input
Automatic Sequence
Controller Test
Controller State Change
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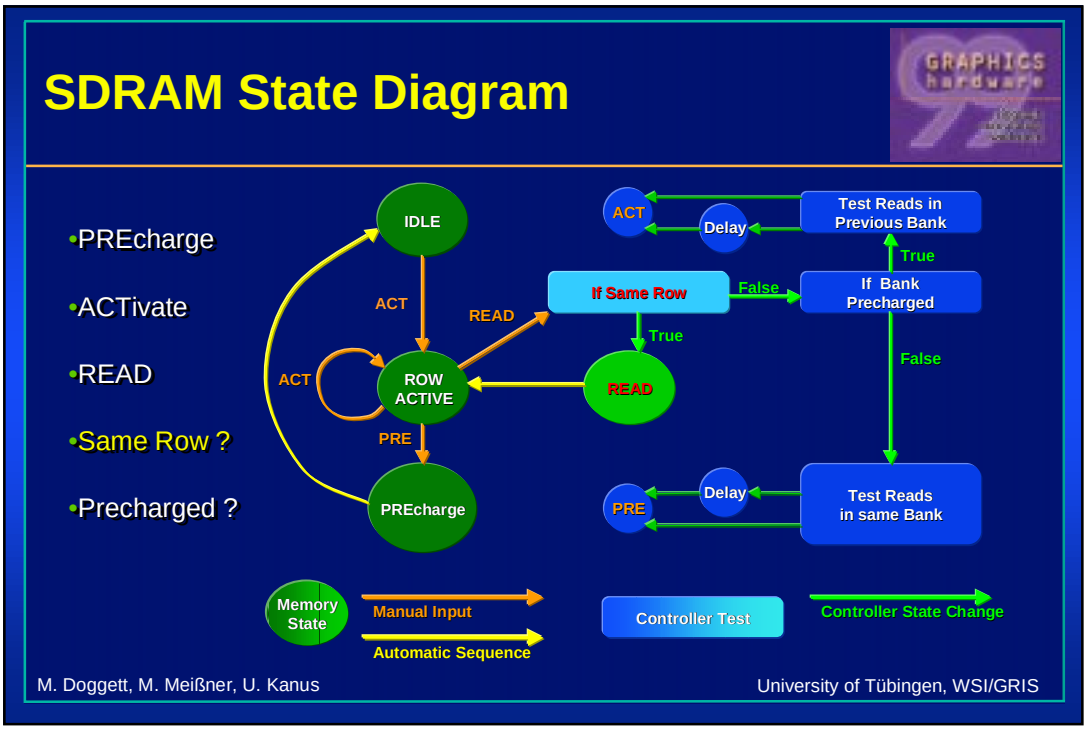
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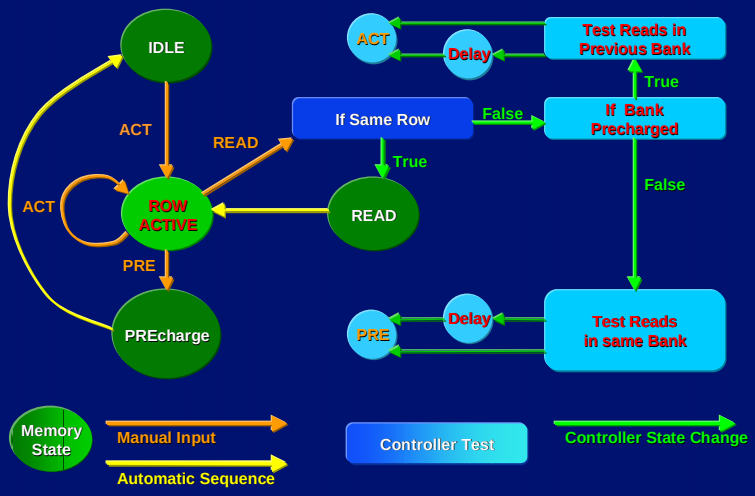
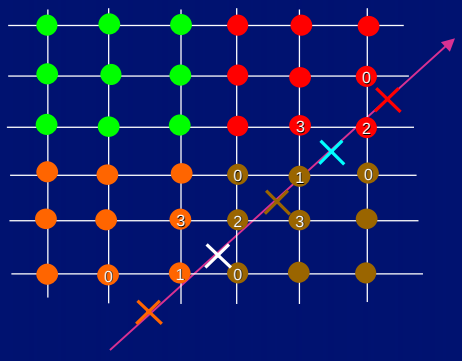


Memory Interface

Cache reloads and pipeline stalls

- 1 - 1 cache
- 2 - 2 caches - 2 reloads
- 3 - 1 cache - 2 reloads
- 4 - 2 caches - 2 reloads
- 5 - 1 cache - 2 reloads

4 pipeline stalls



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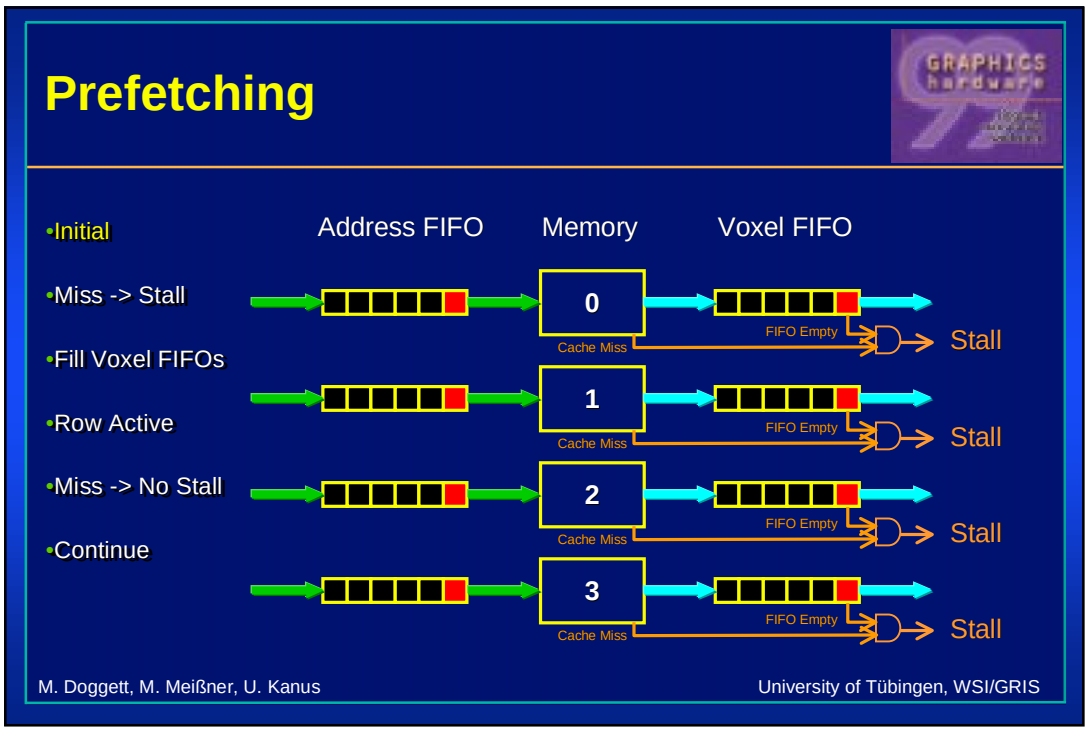

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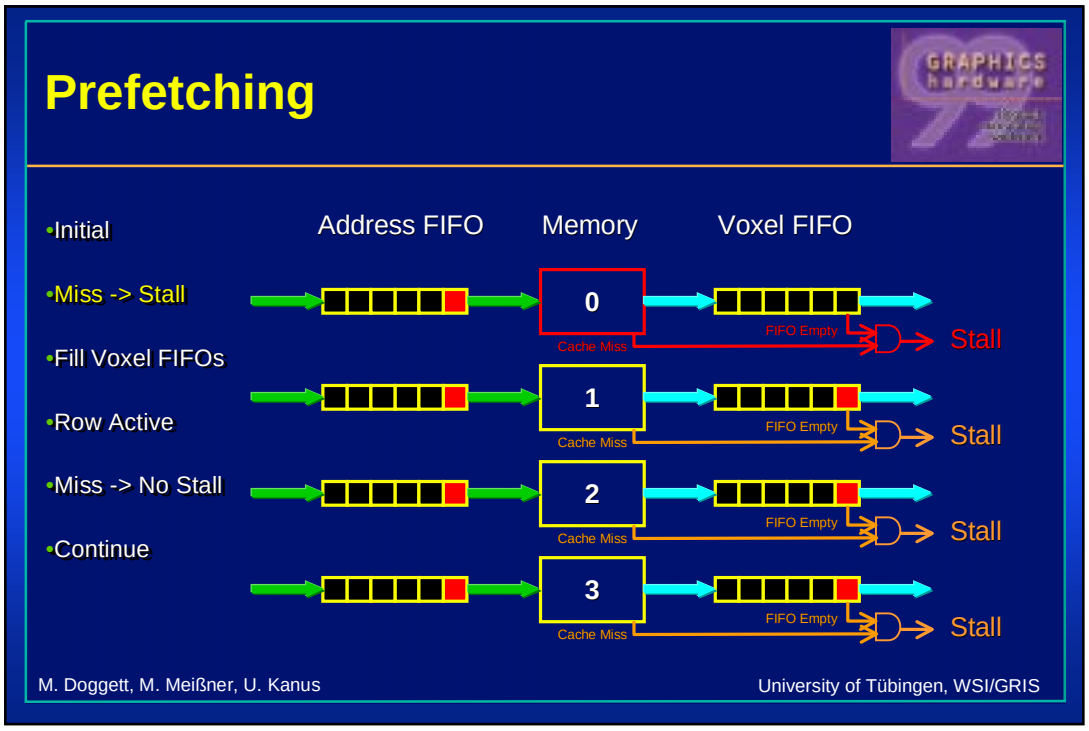

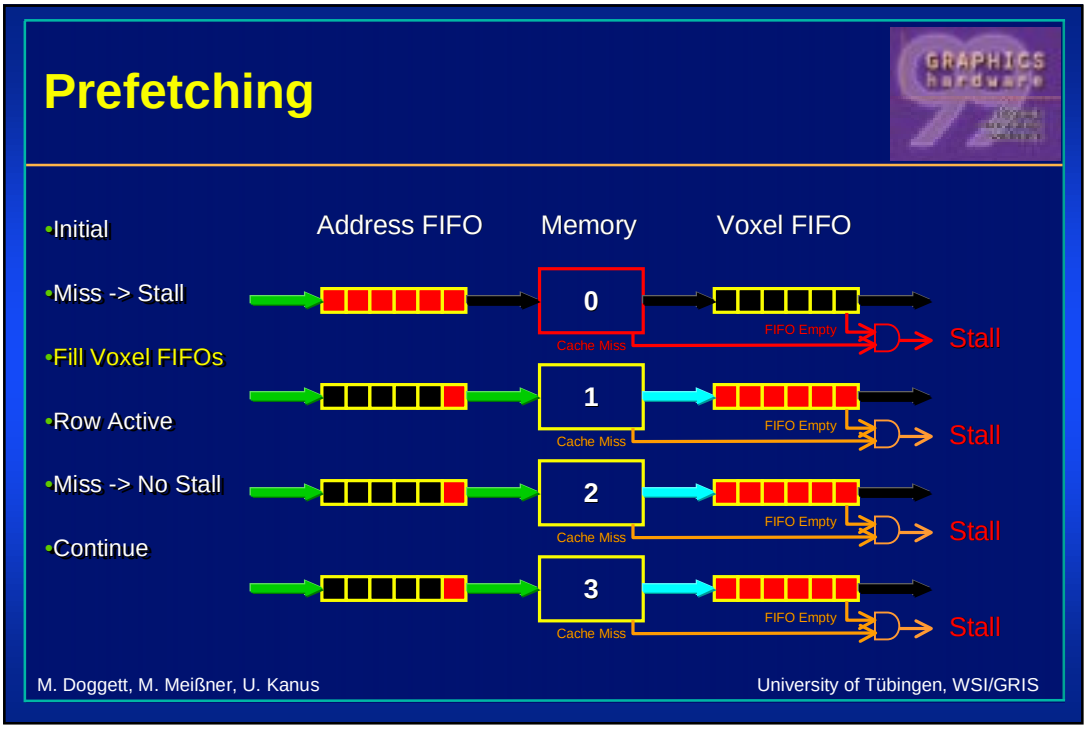
Prefetching
GRAPHICS hardware
•Initial
•Miss -> Stall
•Fill Voxel FIFOs
•Row Active
•Miss -> No Stall
•Continue
Address FIFO
Memory
Voxel FIFO
0
1
2
3
Cache Miss
FIFO Empty
Stall
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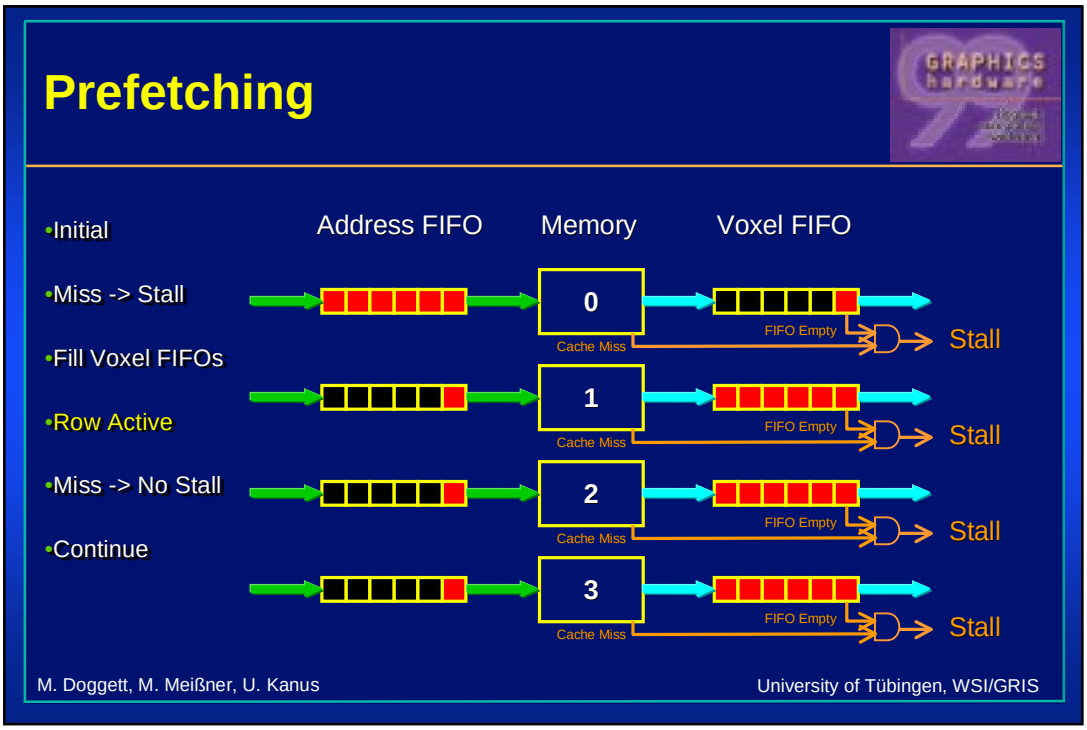
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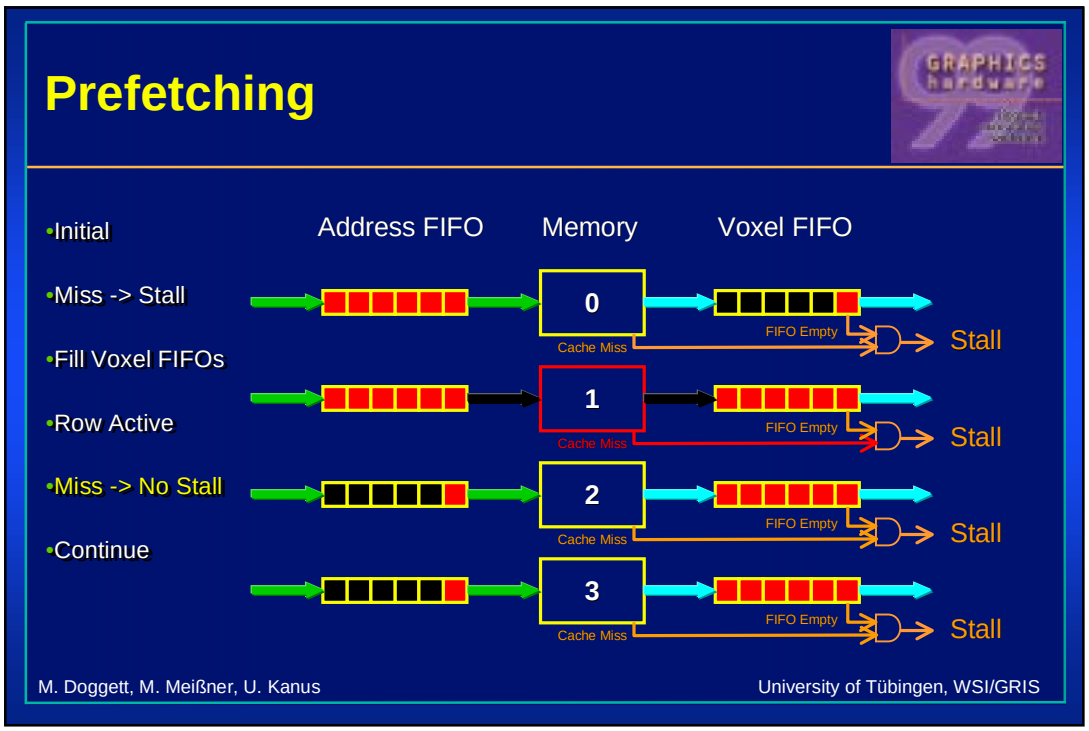

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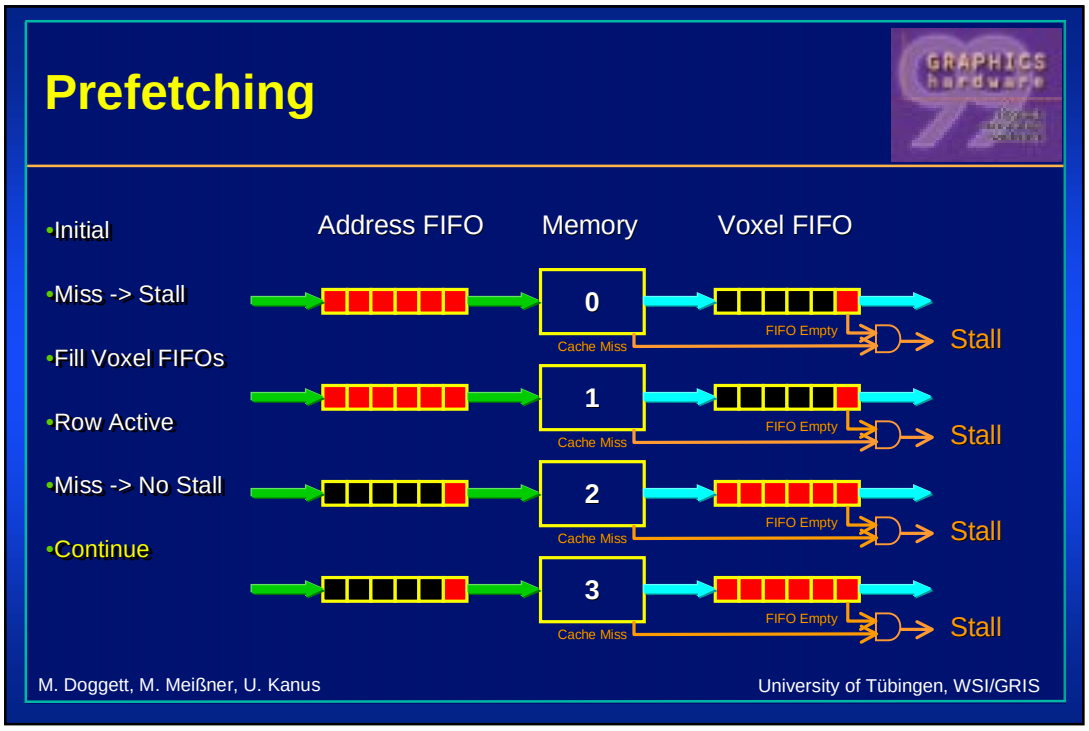

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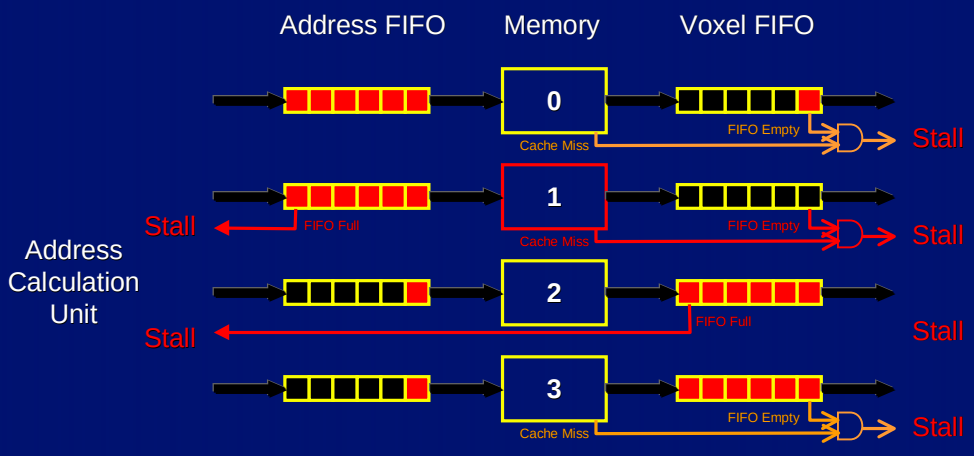

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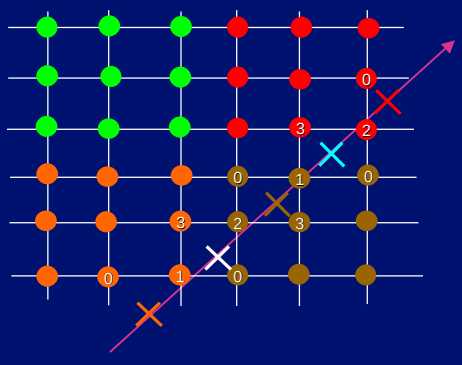
Memory Interface

- 1 - 1 cache
- 2 - 2 caches - 2 reloads
- 3 - 1 cache - 2 reloads - No Stall
- 4 - 2 caches - 2 reloads
- 5 - 1 cache - 2 reloads - No Stall

Only 2 pipeline stalls



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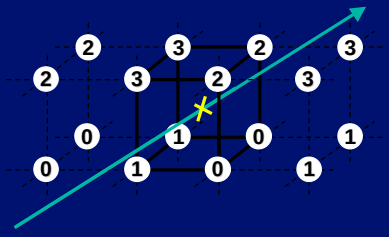
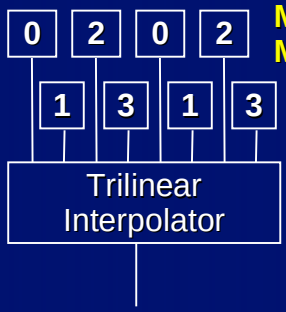
Memory Structures

4 DIMMs

- Off the shelf
- Cheap
- Upgradeable
- Large capacity (up to 1 GB)
- 4 addresses ⇨ Data replication

Memory Interface





Disadvantage - Data replication

Sample

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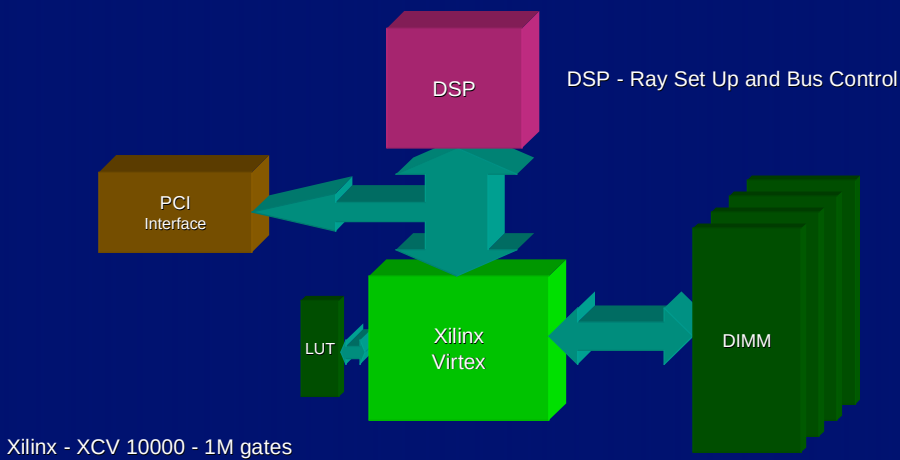
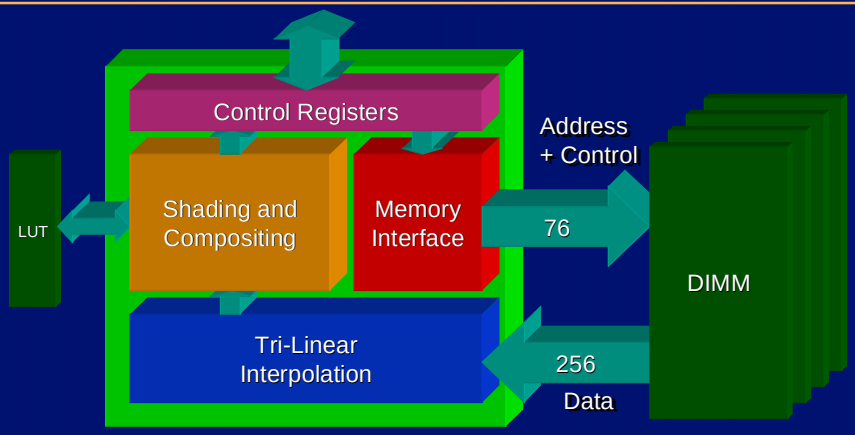
PCI Board



Xilinx - XCV 10000 - 1M gates

Xilinx



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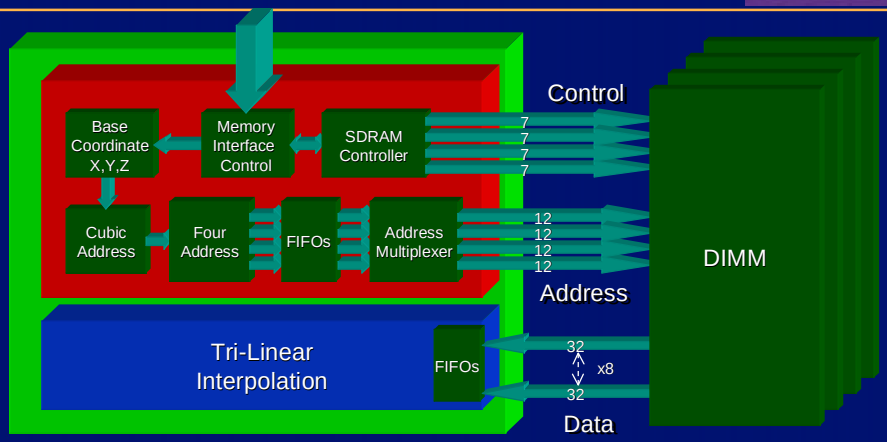
Memory Interface



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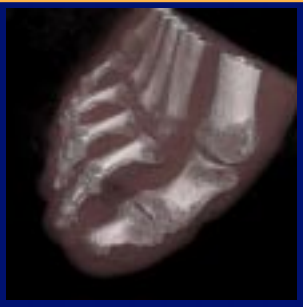
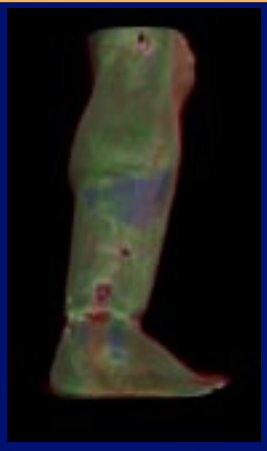
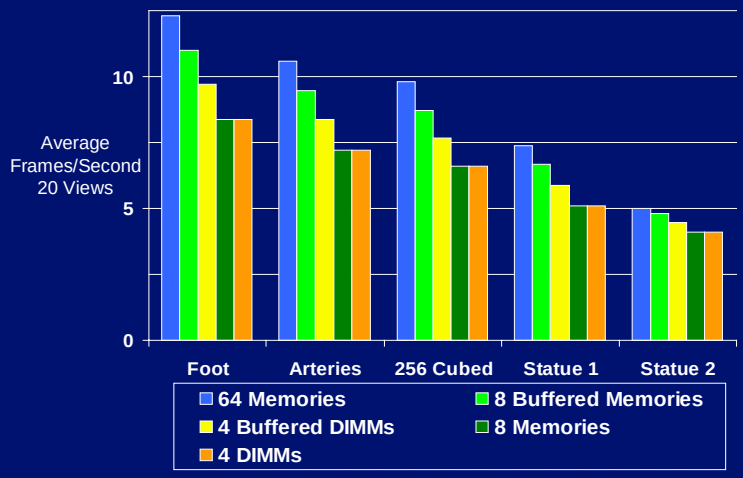


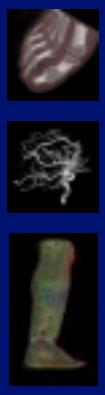


Foot - 256^3
Arteries - 256^3
Statue 1 - 341^2 x 364 (original data 341^2x91)
Statue 2 - Double sampling in view direction

Software Simulation using SDRAM state model and NEC 100MHz SDRAM timings

Results





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VHDL simulation

- Initial image result from mixed structural and behavioural VHDL simulations of VIZARD II

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Conclusion

- Improved memory performance by combining Cubic Addressing and Buffering
- DIMMs are a Cheap, Upgradeable, Large capacity Memory solution
- Memory Interface simulated and synthesised in VHDL for Xilinx technology
- Perspective projection high quality images
- First Prototype expected fall 1999

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